APPLICATION NOTE

AN99068
DESIGNERS GUIDE
EXACT GPS Low Cost Reference Board
(Version 1.0)

Philips
Semiconductors

PHILIPS

DESIGNERS GUIDE **Application Note**

EXACT GPS Low Cost **(Version 1.0)** **AN99068**

Abstract

EXACT is a Philips GPS (Global Positioning System) receiver circuit chip-set comprising an RF front-end, UAA1570HL and a Baseband processor, SAA1575HL. The firmware is supplied with the purchase of the chip-set providing the user with a complete navigation solution capable of accuracies to within 5 meters with the use of Differential GPS (DGPS). The EXACT low cost reference design has been developed to demonstrate a small, low cost, low power GPS receiver solution using the EXACT chip-set. This system is intended as a reference that can be used by the customer to greatly reduce the development time and cost for their own receiver design. The EXACT Designers Guide details every aspect of the reference system design through to PCB layout. Also provided in this document are the full schematics, parts lists and assembly drawings as well as detailed test instructions and a fault finding guide to aid production testing.

Purchase of Philips I^2C components conveys a license under the Philips I^2C patent to use the components in the I^2C system, provided the system conforms to the I^2C specifications defined by Philips.

APPLICATION NOTE

AN99068
DESIGNERS GUIDE
EXACT GPS Low Cost Reference Board
(Version 1.0)

Author(s)

M Thorne

G Addey

Philips Semiconductors Systems Laboratory Southampton, England

Keywords:

GPS
EXACT
PCB
SAA1575
UAA1570

Date: 02 December, 1999

Summary

EXACT is a Philips GPS receiver chip-set, including system firmware, providing the user with a complete navigation solution capable of accuracies to within 5 meters with the use of Differential GPS (DGPS). EXACT is a two chip solution comprising an RF front-end, UAA1570HL and a Baseband processor, SAA1575HL. The EXACT low cost reference design has been developed to demonstrate a small, low cost, low power GPS receiver solution using the EXACT chip-set.The EXACT Designers Guide details every aspect of the reference system design through to PCB layout. Also provided in this document are the full schematics, parts lists and assembly drawings as well as detailed test instructions and a fault finding guide to aid production testing.

Table of Contents **Page Number**

Table of Contents Cont'd **Page Number**

Table of Contents Cont'd **Page Number**

List of Tables **Page Number**

List of Tables cont'd **Page Number**

List of Figures **Page Number**

1 INTRODUCTION

EXACT is a Philips GPS (Global Positioning System) receiver circuit chip-set which will provide the user with a GPS receiver function, as well as an embedded controller to convert the raw satellite data to a navigation solution. The controller is capable of receiving Differential GPS (DGPS) data which will allow position accuracy to be within 5 meters. Philips technology will allow you to think of GPS as what it really is; a general purpose utility that provides position and time information.

This board runs from a 3 V supply allowing very low power operation. It implements a cost optimised design both in terms of external components and board size. The design is typical of OEM modules currently available on the market and serves as an ideal reference layout for the chip-set. This document provides details of the hardware and layout to enable customers to design the chip-set in quickly, by greatly reducing development time.

1.1 Glossary

2D	Two dimensional.
3D	Three dimensional.
Acquisition	The process of finding and locking on to a satellite signal.
A/D	Analogue to Digital Converter.
Almanac	A set of data describing the position of all satellites in the GPS constellation.
BIT	Built In Test.
BPF	Bandpass Filter.
Channel	One of 8 physical hardware receivers available to demodulate a satellite signal.
Channel algorithm	Low level software to manage each channel of the EXACT baseband receiver.
Constellation	The arrangement of the satellites in the sky.
Correlator	A system for computing the correlation of a signal with another local reference.
Datum	A reference set of co-ordinates which defines the model of the surface of the earth used for position computations. The default is WGS-84.
DGPS	Differential GPS.
DOP	Dilution Of Precision, ie: reduction of precision in a computation due to bad satellite geometry.
DRAM	Dynamic RAM.
ECEF	Earth Centred Earth Fixed.
EEPROM	Electrically Erasable Programmable ROM.
Elevation	Angle above the horizon in degrees.
Elevation Mask	Elevation angle above which satellites will be used in navigation computation.

EPROM	Electrically Programmable ROM.
EXACT	England XA Ashtech CPG Technology.
GPS	Global Positioning System.
HDOP	Horizontal Dilution of Precision.
IC	Integrated Circuit.
Icc	Current supplied to the positive terminal of a circuit.
Image Rejection	The attenuation of the image frequency in a mixing process.
I/O	Input/Output.
J/S	Jammer to Signal Ratio
L1	The frequency band for civil GPS signals (centred on 1575.42 MHz).
LNA	Low Noise Amplifier.
Mask	A programmable threshold value above or below which data will not be used.
Navigation solution	High level software to compute the position from received satellite data.
NMEA0183	Standard for transmitting/receiving navigation information.
Noise Figure	The additional noise added by a circuit, over and above that due to the input noise.
PPS	Pulse per second.
PRN	Pseudo-Random Noise (ie: the unique spreading code used per satellite).
RAM	Random Access Memory.
RF	Radio Frequency.
RF Sensitivity	The minimum signal level required to achieve a given level of performance.
ROM	Read Only Memory.
RTC	Real Time Clock.
RTCM-SC104	Standard for differential correction data.
UAA1570	The type number of the RF front-end IC of EXACT.
SAA1575	The type number of the digital baseband IC of EXACT.
Signal Strength	The signal level of the satellite signal on a given channel, as computed by the correlator hardware in the channel.
Spurious	An unwanted signal.
SV	Space Vehicle, ie: a satellite.

TTFF	Time To First Fix.
UART	Universal Asynchronous Receiver Transmitter.
Update Rate	The frequency at which navigation solutions are computed.
UTC	Universal Time Co-ordinated.
VCC	Positive supply voltage.
VDOP	Vertical Dilution of Precision.
VSWR	Voltage Standing Wave Ratio (a measure of quality of matching of impedance).
WGS-84	A datum, World Geodetic System 1984.

1.2 Features

- Eight parallel satellite channels tracking eight satellites at the same time.
- Power Management functions.
  Power down mode.
  Reduced update rate option.
- Supports true NMEA 0183 data protocol.
- Direct differential RTCM SC-104 capability.
- Rapid Time-To-First-Fix (TTFF).
- RF input designed for active or passive Antenna Systems.
- Multiple Operating Modes.
  Automatic Mode.
  Fixed 3D mode.
  Fixed 2D mode.

  In all the above modes, UTC time is also available.
- User programmable Elevation Mask.[1]
- User programmable DOP Masks.[1]
- User programmable Satellite signal level mask. [1]
- Standard serial I/O.

1. The software provided defaults to selected values to optimize performance, but each parameter is user programmable.

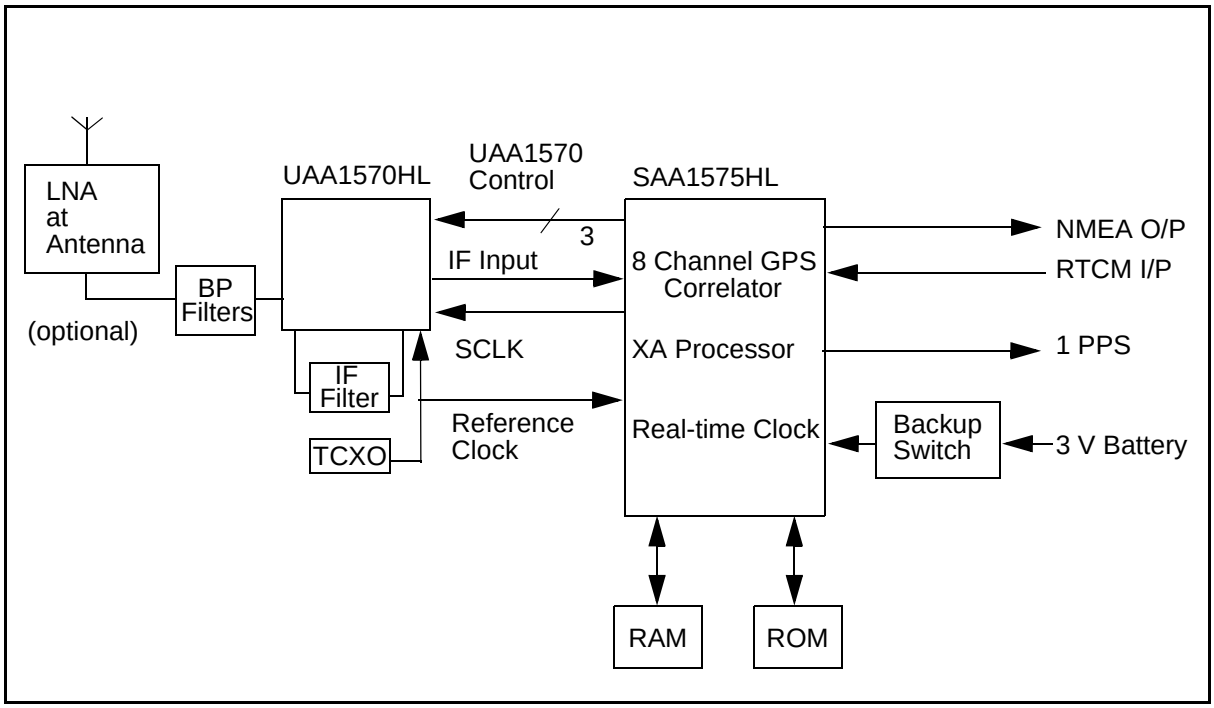


Figure 1 Simplified Block Diagram

2 PRODUCT DESCRIPTION

The EXACT Low Cost Reference Board has been designed primarily to reduce system cost, and provide a reference layout for a typical OEM type module. It runs directly from a 3 V DC supply and provides a TTL interface for both UARTS. The battery backup supply must be provided externally as well as the antenna supply input. This enables the use of either 5 V or 3 V active antenna in the application. The system described is intended for use with an active GPS antenna with between 10 dB and 26 dB gain including cable losses.

The description outlined in the following sections is specific to this particular application and does not form the total specification of the chip-set. For chip-set specifications please refer to the relevant data sheets, Reference [1] and [2].

2.1 TECHNICAL SPECIFICATION

Table 1 and 2 list the important technical specifications for the system. The total system comprises two PCB's the first being the GPS Engine and the other the GPS Mother-board. The GPS Engine provides the complete GPS solution and provides a 3 V CMOS interface for the serial ports. The GPS Mother-board primarily provides both the system and backup power for the GPS Engine as well as RS232 compliant outputs for interface to a standard PC serial port(s).

Table 1 Technical Specification for the GPS Engine

Item	Specification
General	8-Channel continuous tracking GPS Receiver Board
GPS Parameters	L1 Frequency, C/A code (SPS)
Update Rate	User Programmable Between 1 second and 999 seconds (Default = 1 second)
Communication Interface	Standard NMEA-0183 V2.1 Output Supports RTCM-SC104 message types 1,3,6,9 and 16 for DGPS Input
Serial Ports	One TTL full duplex for standard I/O One TTL half duplex for RTCM Input
Baud Rate	User programmable between 300bps to 19200bps. Maximum recommended character rate is 400 characters per second
Board Dimensions	Bare Board: 2.29 x 1.72 x 0.06 Inches (58.2 x 43.7 x 1.6 mm) Populated: 2.29 x 1.72 x 0.79 Inches (58.2 x 43.7 x 20 mm)
Board Connector	20 Way Header 0.1" Pitch (Dual 10 way)
Input Voltage	System Supply 3 V± 5%
Input Power	3 V DC < 320 mW typical
Backup Voltage	2.7 to 3.1 V (Typically 3 V Lithium cell)
Backup Power	3 V DC < 40 μW typical (13 μA)
Noise Figure	7 dB typical without antenna

Table 2 Technical Specification for the Mother-Board

Item	Specification
General	Provides power regulators and RS232 interface for GPS Engine
Indicators	LED Indicators for 3 V, 5 V supplies and 1PPS Output
Antenna Supply	Switchable between 3 and 5 V
Battery Backup	3 V Lithium Backup. Switchable to be on or off
Serial Ports	2 Off 9-Way Male D-Types
Master Reset	Push button switch provided to force complete system reset
Board Dimensions	Bare Board: 4.06 x 3.58 x 0.06 Inches (103 x 91 x 1.6 mm) Populated: 4.06 x 3.58 x 0.98 Inches (103 x 91 x 25 mm)
Input Voltage	Supply input via molex type connector or standard DC adaptor Voltage Input Between 7 and 17 V DC

2.2 Performance Specification

Table 3 summarises the main performance specification for the GPS System.

Table 3 Performance Specifications

Item	Specification
Autonomous Position Accuracy	Horizontal 95% 100 m (**Typically 50 m**) Vertical 95% 156 m Speed 0.2 km/h
DGPS Accuracy	Horizontal 95% 10 m (**Typically 5 m**) Vertical 50% 6.5 m Speed 0.1 km/h
Typical Acquisition Time	< 10 secs HOT (Valid ephemeris, almanac, last pos' and time) < 45 secs WARM (Valid almanac, last pos' and time) < 120 secs COLD (No valid data held)
Typical Reacquisition Time 50%	< 1 sec (Complete satellite blockage < 10 seconds) < 3 secs (Complete satellite blockage < 60 seconds) < 10 secs (Complete satellite blockage < 600 seconds)
Update Rate	User selectable from 1 second to 999 seconds in 1 second increments synchronised with GPS.
1PPS Output	Calculates time and outputs a 1PPS pulse when it has a position and is tracking one or more satellites. 1PPS output is synchronised to GPS time ± 1 μS.

2.3 Antenna Specification

For this board the VIC1 active antenna by Matsushita Electric Works, MEW, has been implemented. This is a fairly typical active antenna intended for in vehicle GPS applications. It is important that the antenna gets a clear view of the sky and is positioned on a surface level to the horizon for best results. The following specification is typical for use with the EXACT low cost reference design.

Table 4 Typical Active Antenna Characteristics

Characteristic	Specification
Polarisation	Right-Hand Circular Polarised
Receiving Frequency	1.57542 GHz ± 1.023 MHz
Power Supply	+3 to +5 V
DC Current	< 15 mA @ 3 V < 50 mA @ 5 V
Total Gain	+13 dBi to +26 dBi
Output VSWR	< 2.5

The Matsushita Electric Works, VIC1 antenna is a 5 V, 20 mA, active antenna with 26 dB gain.

Part No: GPS-F-26-SMA-01-B Manufacturing No: CCAD20KG01

A good alternative to the Matsushita antenna is the 3900 range from SiGEM. These antenna can be operated over a wide voltage range, nominally 3 to 5 V, and exhibit very low current and Noise Figure.

1. SGM3900 I = 7 mA @ 3 V, G = 28 dB, NF = 0.8 dB

2. SGM3902 I < 5 mA @ 3 V, G = 13 dB, NF = 1.4 dB.

2.4 Electrical Connections

A 20 way interface is provided on this board allowing general purpose lines to be used externally if required. In practice this could be reduced if required to minimise connector size. Table 5, lists the assigned signal connections for the board.

Table 5 EXACT Low Cost Reference Board Connector Pin Assignments

Pin #	Signal Name	Description
1	VANT	Antenna Supply (Switchable from mother-board between 3 and 5 V)
2	VRF	3 V RF Supply Input
3	VBATT	Battery Backup Supply Input
4	RF GND	GND For RF Supply
5	MRESET	Master Reset Input (Active Low)
6	GPIO0	General Purpose I/O from SAA1575 (Port 0)
7	GPIO1	General Purpose I/O from SAA1575 (Port 1)
8	GPIO2	General Purpose I/O from SAA1575 (Port 2)
9	GPIO3	General Purpose I/O from SAA1575 (Port 3)
10	DIG GND	GND for Digital Supply
11	TXD0	1st Transmit Output from SAA1575
12	RXD0	1st Receive Input to SAA1575
13	DIG GND	GND for Digital Supply
14	TXD1	2nd Transmit Output from SAA1575
15	RXD1	2nd Receive Input to SAA1575
16	DIG GND	GND for Digital Supply
17	NC	This pin not used
18	DIG GND	GND for Digital Supply
19	1PPS	One Pulse Per Second output pin from SAA1575
20	3 V DIG	Main 3 V Digital Supply Input

2.5 EXACT GPS Mother-Board

To enable the GPS Engine to be interfaced easily with a PC, and/or field tested, a mother-board has been developed which accommodates the GPS board. The mother-board provides 2 power connectors to allow drive from either a bench power supply or by mains power adaptor. It will accept a DC input between 7 and 17 V and regulate down to both 5 and 3 V. The 5 V regulator is used to provide an alternative power source for an active antenna.

This board also converts the 3 V CMOS levels to true RS232 levels for interfacing with a PC and provides a lithium cell for battery backup operation. The power source for the antenna can be switched between 5 and 3 V and the battery backup facility can be enabled or disabled by a toggle switch. Two male 9 way D-Type connectors are provided allowing interface to a PC via a standard 9 way null modem cable assembly.

Full details of the mother-board can be found in Section 5 on Page 73.

2.6 GPS Engine PCB

This section provides a physical overview of the EXACT Low Cost Reference System.

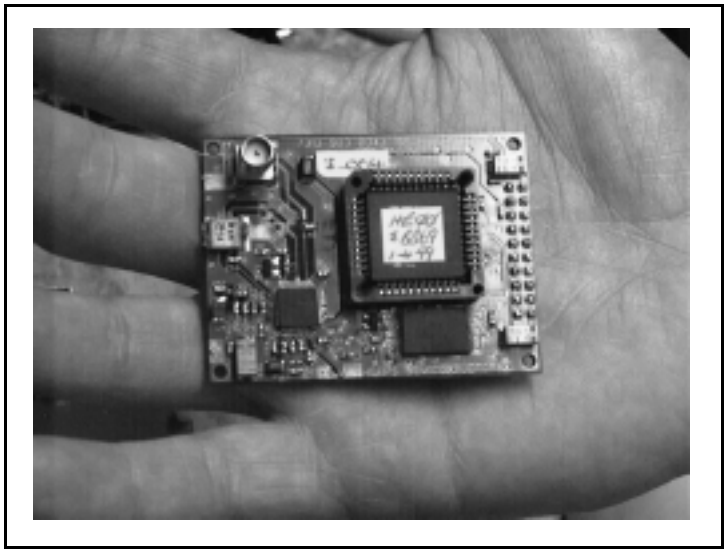


Figure 2 Picture of the EXACT Low Cost Reference Board (GPS Engine)

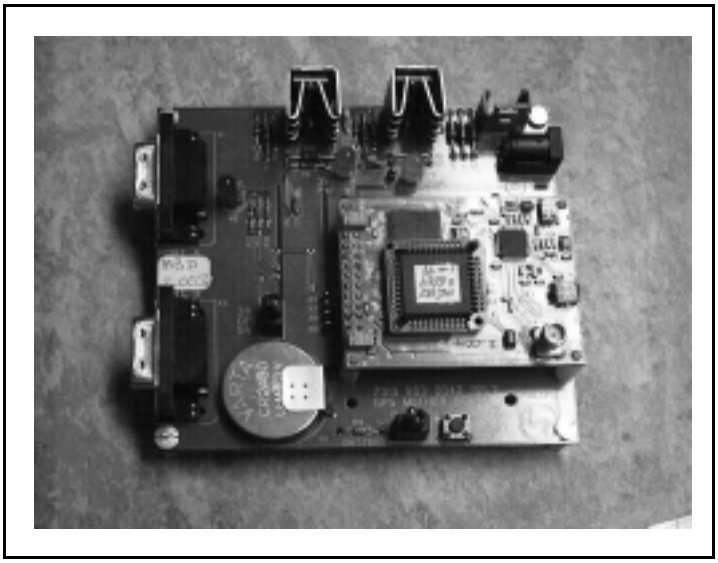


Figure 3 Picture of the Complete EXACT Low Cost Reference System

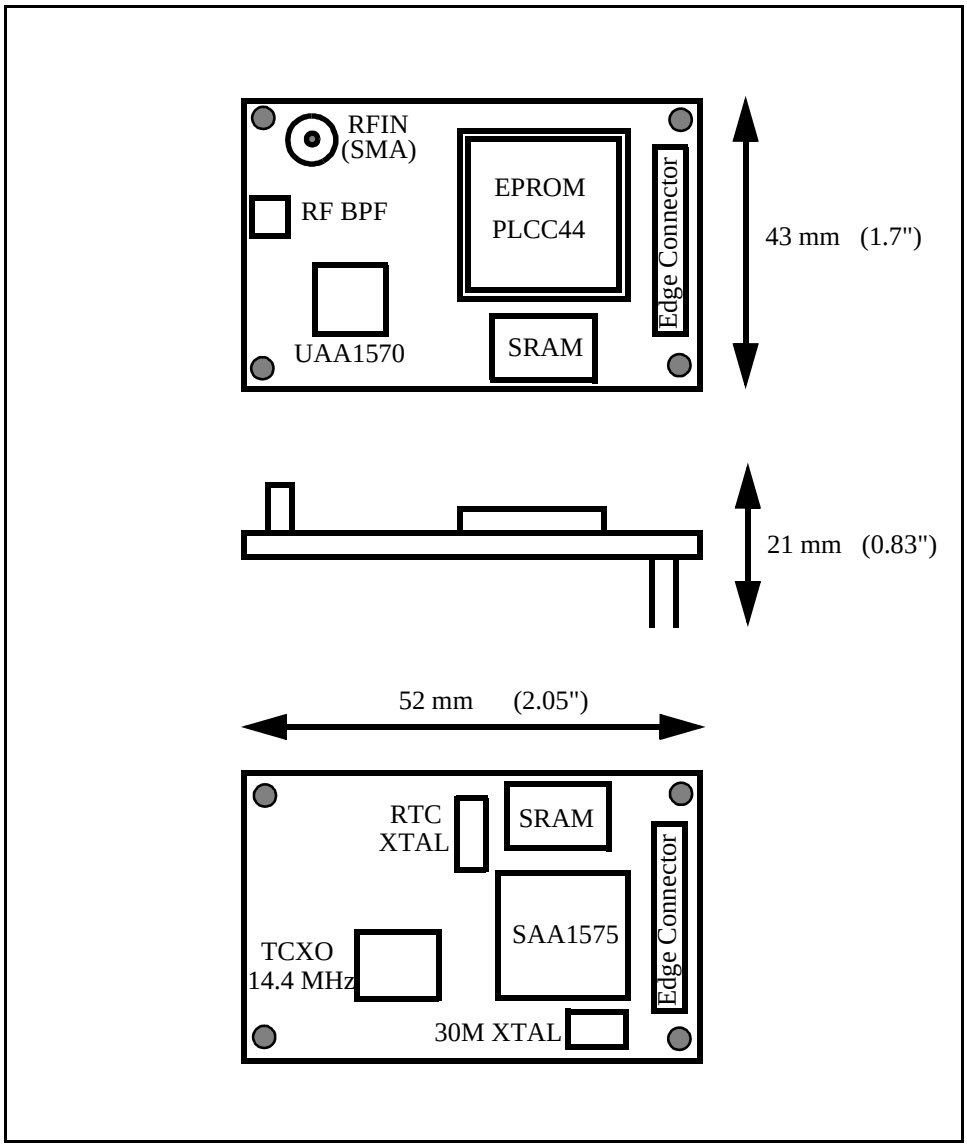


Figure 4 Overview of GPS Engine Board

The GPS Engine PCB is constructed from 4 layers using standard FR4 dielectric. For all microstrip line calculations a dielectric constant, Er, of 4.0 has been used which falls somewhere between a typical range of 3.8 to 4.2. The design of the microstrip matching lines and various calculations used can be found in Section 3.2 on Page 22.

3 GPS ENGINE DESIGN GUIDE

This section provides detailed design information related to the EXACT chip-set application. Each block of the EXACT GPS system is covered in turn, explaining the basic functionality and highlighting the critical areas of the design.

3.1 GPS Antenna Selection

The reference system described in this manual has been designed for use with an active GPS antenna. The antenna used depends upon the implementation of the embedded LNA's on the UAA1570. This section describes the various possible combinations and associated antenna types that can be used, including passive antenna implementation.

3.1.1 Passive Antenna Solution

When a passive antenna is to be used both on chip LNA's must be implemented to maximise the RF gain in the system. This application is generally the most difficult to achieve as in most cases the other goal in the system is small size. Typical passive patch antenna require a significant ground plane area to optimize gain and system Noise Figure. Table 6 gives an overview of the various constraints.

Table 6 Requirement Specification for Passive Antenna

LNA's Implemented	Maximum External Gain	Minimum External Gain	Maximum Ext Noise Figure	Minimum GND Plane Area
LNA1 & LNA2	10 dB	2 dB	3.5 dB	50 mm X 50 mm

The figures given in Table 6 are those recommended, including all cable and filter losses, and do not represent absolute system limits. For example if in this case an active antenna was used with greater than 10 dB of gain, the system would in many cases still function. The problem is that if great care is not taken to protect the RF stages from the antenna itself, feedback can occur resulting in instability in the system. Alternatively it may be possible to use a passive antenna with a typical gain at the zenith of 0 dB, but in this instance the layout and performance of the RF stages would be extremely critical. If the system gain and Noise Figure was not optimal throughout then problems may be encountered. We strongly advise that only high gain passive, ground-planed antenna are used in these applications with nominal gain at 1.57542 GHz of at least 4 dB to 5 dB at the zenith.

Many typical passive elements on the market exhibit gains of around 4.5 dB, when implemented with an associated ground plane of 70 mm X 70 mm. This size of ground plane is invariably an obstacle in many applications where size is major factor of the design. It is recommended that at least 2 dB of gain is realised by the antenna element to ensure successful system performance. To achieve this the ground plane arrangement is absolutely critical. One of the fundamental problems with passive antenna is that the ground plane area and implementation affects the centre frequency resonance tuning. Therefore if the manufacturers ground plane specification is not followed the antenna element will be detuned and consequently the gain at the desired centre frequency is degraded. It is advisable to evaluate the chosen element with various ground plane configurations to establish suitable gain realisation prior to designing the PCB itself. **If the element gain is not realised it is almost impossible to recover the consequences of it in the latter stages of the RF design**.

The mounting of the antenna is also a major consideration here. Ideally the antenna should be mounted offset to the PCB, that is to one side, with suitable ground plane arrangements. An alternative to this is to isolate the antenna with very short cable length. In both cases the RF sections of the PCB itself should be shielded to prevent any feedback resulting from the close proximity of the patch itself.

3.1.2 Active Antenna Solutions

In applications intending to use active GPS antenna either one or both of the on-chip LNA's from the UAA1570 will be bypassed. More commonly a single LNA will be used together with a typical active antenna with gains in the region of 13 dB to 26 dB. In instances where active antenna gain is greater than 26 dB it is recommended to bypass both LNA's. Table 7 gives an overview of the constraints.

Table 7 Requirement Specification for Active Antenna

LNA's Implemented	Maximum External Gain	Minimum External Gain	Maximum Ext Noise Figure
Single LNA [1]	26 dB	8 dB	3.5 dB
Both LNA's [1 & 2]	41 dB	23 dB	3.5 dB

1) The maximum external NF listed is that which will produce approximately 1 dB degradation in system NF using the minimum recommended external gain. The maximum recommended external gain could result in approximately 1 dB compression in the second mixer input with an in-band continuous wave jammer present (J/S = 35 dB) for normal processed parts.

2) If a high gain external LNA is used both LNA1 and LNA2 should be removed from the signal path. However, the LNA2 supply must still be connected to Vcc to retain power to the first mixer.

The figures given in Table 7 are those recommended, including all cable and filter losses, and do not represent absolute system limits. Whenever an active antenna is used it is suggested that its placement is reasonably clear of the RF stages of the PCB to prevent an chance of feedback and instability as a result. It is recommended that the RF stages are shielded to protect them from any external interference effects.

3.1.3 Circuit Considerations for Disabling On-Chip LNA's

When at least one of the on-chip LNA's from the UAA1570 are to be bypassed it is important to ground the associated input pin and leave the output pins open circuit. In all cases VCCLNA2 must be connected to the main supply but VCCLNA1 can be left open circuit if LNA1 is bypassed. In typical 3 V applications disabling one or both on-chip LNA's will save around 6.5 mA of supply current. In a single LNA application it is recommended that LNA2 is implemented and LNA1 bypassed to save current.

For manufacturer details of various passive and active antenna for GPS refer to Section 9.6 on Page 107.

3.2 Impedance Matching for RF Stages

The RF inputs and outputs must be matched to a 50 Ohm environment using either microstrip line design or L and C matching circuits. Table 8 on Page 23 provides the matching impedances of all the RF input and output pins of the UAA1570 at the L1 frequency of 1.57542 GHz. In the reference design microstrip lines have been implemented to minimise external components, but if preferred the matching could also be done using L and C networks.

Table 8 RF Matching Impedances (1.57542 GHz)

Function	UAA1570 Pin Number	Real Part	Imaginary Part
LNA1 Input	45	31	- j32
LNA1 Output	48	77.5	+ j6
LNA2 Input	3	24	- j25
LNA2 Output	6	74.5	- j0.5
Mixer1 Input	14	33.5	-j25.5

The EXACT Low Cost Reference Board Design utilises LNA2 only and the matching design for these pins are detailed in this section. The same design principle would apply if LNA1 was also to be implemented and for completeness the matching networks suggested for these pins are also included.

In each case a netlist of the matching circuit as well as component and trace properties is included. Table 9, below helps to understand what the netlist represents in physical terms.

Table 9 Netlist Parameters Description

CAP **TLIN**	**2 0**	**C = 0.25** **E = 34.50**
CAP = Capacitor RES = Resistor TLIN = Microstrip Line TLOC = Open Stub Microstrip	Circuit Nodes (ie: between nodes 2 and 0)	Capacitance in pF Resistance in Ohms Electrical Length in Degrees Electrical Length in Degrees

The matching circuits were designed with the following goals:

Magnitude of Reflection Coefficient -18 dB to -15 dB

Voltage Standing Wave Ratio (VSWR) 1.28 to 1.43.

3.2.1 Microstrip Design Procedure

This section details the design approach used to produce the matching networks for the EXACT Low Cost reference Board. In order to minimise component count a microstrip approach was taken as opposed to using Inductor and Capacitor tuning networks. The latter makes on board tuning easier after manufacture provided track lengths are kept fairly short, but with care the microstrip approach provides a cheap and accurate solution.

The design approach uses standard formulae and requires the use of a Smith Chart either in paper form or in this case a software program, EEZMatch. Details on how to obtain this software can be found in Section 9.7 on Page 108.

3.2.1.1 determining track widths

The track width used to tune the network needs to be chosen such that it is wide enough to avoid any tolerance effects in production but at the same time able to be long enough to provide adequate interconnect between components. There are a number of detailed formulae available to determine impedance for given track widths and a simplified one is provided here as an example. In most cases the board manufacturer will be able to tune the line impedances to your requirements if you specify beforehand what tracks need to be impedance controlled. In this case a 4 layer board was used as detailed in Figure 5.

The board uses FR4 dielectric with a Dielectric constant, Er, of around 4.0.

Copper Thickness was specified at 0.035 mm.

Characteristic Line Impedance chosen at around 100R.

Characteristic Impedance of bias line chosen at nominally 78R. This was chosen as a compromise between minimum size and short circuit current handling.

Given all these details it is now possible to determine the required track width to achieve the target line impedances used for the various Rf networks.

.

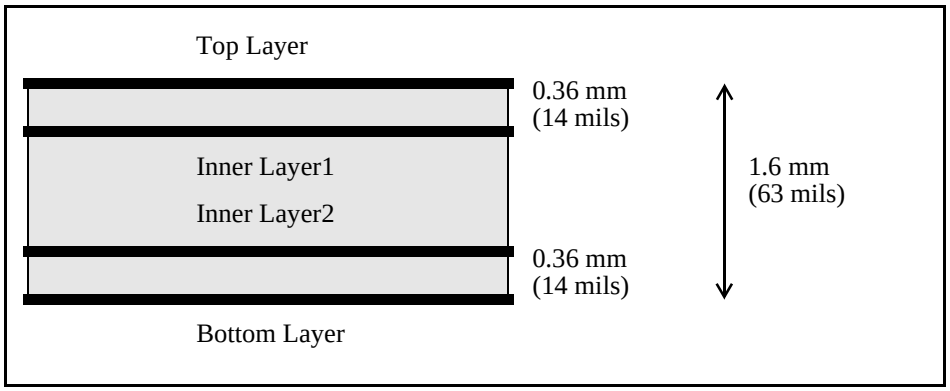


Figure 5 Layer Construction for GPS Engine Board

The following equations can be used;

$$W = 1.25 \times (((5.98 \times D) / 10^{((Zo)/(201/(\sqrt{Er + 1.41})))}) - 2C)$$

Equation: Calculation of track width for given characteristic impedance, Zo.

$$Zo = ((201/(\sqrt{Er + 1.41})) \times \log((5.98 \times D)/((0.8 \times W) + 2C)))$$

Equation: Calculation of characteristic impedance for given track width, W.

These equations generally give results more closely matched to those specified by our PCB manufacturer for track impedances of 50 Ohms or more. In general it is recommended that these formula are only used as a guide and ultimately the impedance objectives should be discussed with each specific manufacturer who will be able to tune their process to meet your objectives.

A description of the variables used and the final values these equations provide are shown in Table 10 and 11.

Table 10 Track Width Calculations for Impedance Controlled Lines

Description	Label	Value
Dielectric Constant of PCB	Er	4
Distance From Microstrip to Inner GND plane	D	0.3556 mm (14 mils)
Copper Thickness of Track	C	0.035 mm (1.4 mils)
Calculated Track Width for 100 Ohm	W_{100}	0.102 mm (4 mils)
Calculated Track Width for 78 Ohm	W_{78}	0.229 mm (9 mils)
Calculated Track Width for 50 Ohm	W_{50}	0.609 mm (24 mils)
Calculated Track Width for 35 Ohm	W_{35}	1.270 mm (50 mils)

Table 11 Impedance and Velocity Factor for Microstrip Line Calculations

Microstrip	Impedance (Zo)	Velocity Factor (B)
W = 4 mils	99.21 Ohms	3378 Deg/m
W = 9 mils	79.74 Ohms	3485 Deg/m
W = 24 mils	50.31 Ohms	3615 Deg/m
[a]W = 50 mils	33.17 Ohms	3772 Deg/m

a. Calculated by alternative method to that outlined in this Report

When modelling the matching network with EEZMatch, it is necessary to enter the microstrip line lengths in angular distance. To do this we need to be able to calculate the velocity factor of the given line in degrees/metre. The following equations can be used to get an estimate of this ratio. These equations provide a typical expectation and do not take into account the effects imposed by shielding the board. However if the height of the shield is considerably greater than the distance between the associated layers of the PCB, ie: 5 to 10 times, then this effect is very small.

Equation [1] Velocity Factor (Degrees/Metre)

$$\beta = (2 \times \pi)/\lambda$$

Equation [2] Wavelength Constant

$$\lambda = c/(\mathrm{Freq} \times \sqrt{\varepsilon re})$$

Where c = 299792458 m/s Speed of Light

Frequency = 1.57542 GHzGPS Signal Frequency

Er = 4 Typical Dielectric Constant for FR4

Equation [3] Effective Dielectric Constant

$$\varepsilon re = ((\varepsilon r + 1)/2) + ((\varepsilon r - 1)/2) \times F)$$

Equation [4] Height and Width Scaling Factor (For w/h < 1)

$$F = 1/((\sqrt{1 + (1.2 \times h/w)}) + T)$$

Equation [5] Height and Width Scaling Factor (For w/h > 1)

$$F = 1/(\sqrt{1 + (1.2 \times h/w)})$$

Equation [6] Scaling Factor T (When track width < distance between layers)

$$T = 0.04 \times (1 - (w/h))^2$$

3.2.1.2 determining track lengths

Taking a typical example the equations provided above should yield a velocity factor of 3378 Degrees/ metre for the following impedance controlled line.

Track Impedance	100 Ohms
Distance between layers (h)	14 mils (0.2556 mm)
Track Width (w)	4 mils (0.1016 mm)
Dielectric Constant (Er)	4.0.

At this stage EEZMatch can be used to model the matching network entering impedance line lengths in angular degrees. Once the network is correct the angular length can be converted to metres using the velocity factor calculated earlier.

Example: If line length was chosen at 45 degrees

Track Width = 4 mils (100 Ohm) Velocity Factor 3378 Deg/m

Therefore Track Length is 45/3378 = 0.0133m (13.3 mm).

Note: *In practice the matching networks for the reference design were derived using a number of alternative formulae, including those described here. An average between these results and those provided by the PCB manufacturer were used in the final design. Therefore the calculations provided, although closely matching the final design, are not always identical to those used in the final design. However these differences are reasonably small compared to the nominal 10% working practices of the PCB manufacturer and should not have a significant impact on the system performance.*

3.2.2 DC Bias Line Matching Circuit

The bias line is required only where an active antenna is to be used and provides a DC supply to power the antenna but represents an open circuit load condition at the frequency of operation, 1.57542 GHz. The 10 Ohm series resistor has been chosen arbitrarily to limit the current on the line to around 50 mA for a 5 V supply ± 10%.

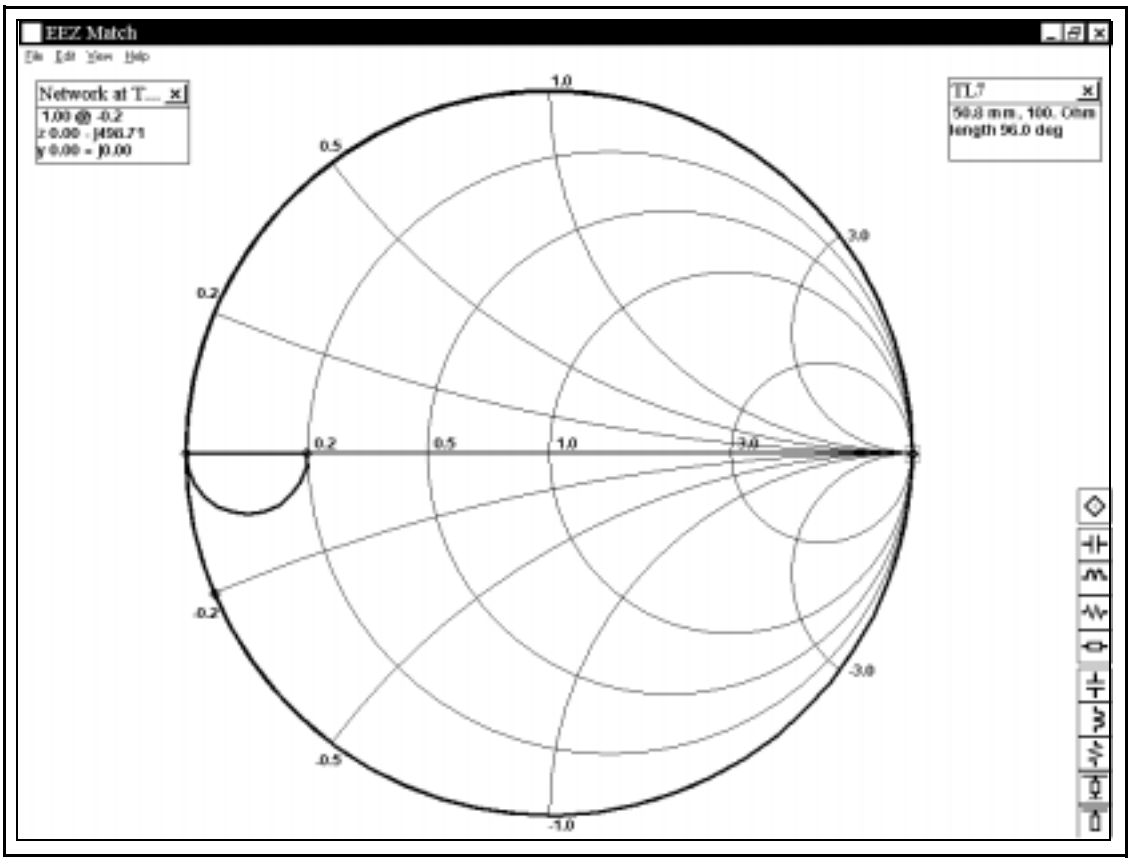


Figure 6 Smith Chart Plot of Bias Line Matching Network

Netlisting for Bias Matching Circuit:

RES 6 15 R=10.0	R1 R = 10 Ohm
CAP 15 0 C=33000.0	C20 C = 33 NF
TLIN 15 16 Z=78.0 E=90.0 F=1.575	(Length E = 91 degrees)
CAP 16 0 C=10.0	C21 C = 10 pF
TLIN 16 17 Z=78.0 E=97.0 F=1.575	(Length E = 98 degrees)

In this network the line width is chosen at 9 mils to provide a characteristic impedance of 78 Ohms. In the network above the line lengths were chosen at 90 degrees and 97 degrees.

Taking the velocity factor calculated above can determine the physical lengths of these lines as follows:

Microstrip Lines (Z ~ 78R)

Electrical lengths of 90 Degrees and 97 Degrees, Velocity Factor = 3485,

L90 Deg = 90/3485 = 26 mm or 1017 mils (27 mm actually implemented)

L97 Deg = 97/3485 = 28 mm or 1096 mils (29 mm actually implemented)

For explanation of differences between the calculated results, and those implemented on the board, (see note Section 3.2.1.2 on Page 26).

3.2.3 LNA2 Input Matching Circuit

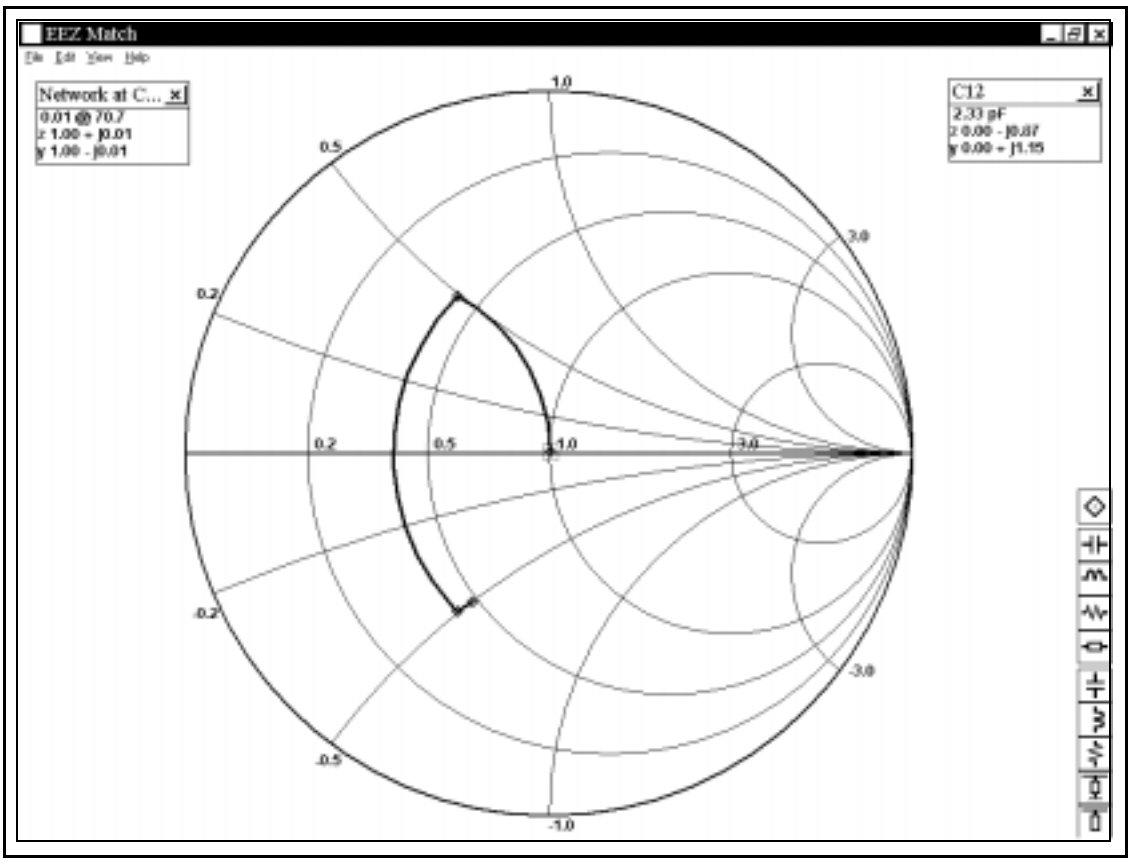


Figure 7 Smith Chart Plot of LNA2IN Matching Network

EEZ Match Network:

CKT

CAP 1 0 C=0.25	C1 C = 0.25 pF (Modelled pin stray capacitance)
TLIN 1 2 Z=100.0 E=29.0 F=1.575	(Length E = 29 Degrees)
CAP 2 0 C=2.3	C2 C = 2.3 pF

In this network the line width is chosen at 4 mils to provide a characteristic impedance of 100 Ohms. In the network above the line length was chosen at 29 degrees.

Taking the velocity factor calculated above can determine the physical lengths of these lines as follows:

Microstrip Line (Z ~ 100R)

Electrical lengths of 29 Degrees, Velocity Factor = 3378,

L29 Deg = 29/3378 = 8.6 mm or 339 mils (8.9 mm actually implemented)

For explanation of differences between the calculated results, and those implemented on the board, (see note Section 3.2.1.2 on Page 26).

3.2.4 LNA2 Output Matching Circuit

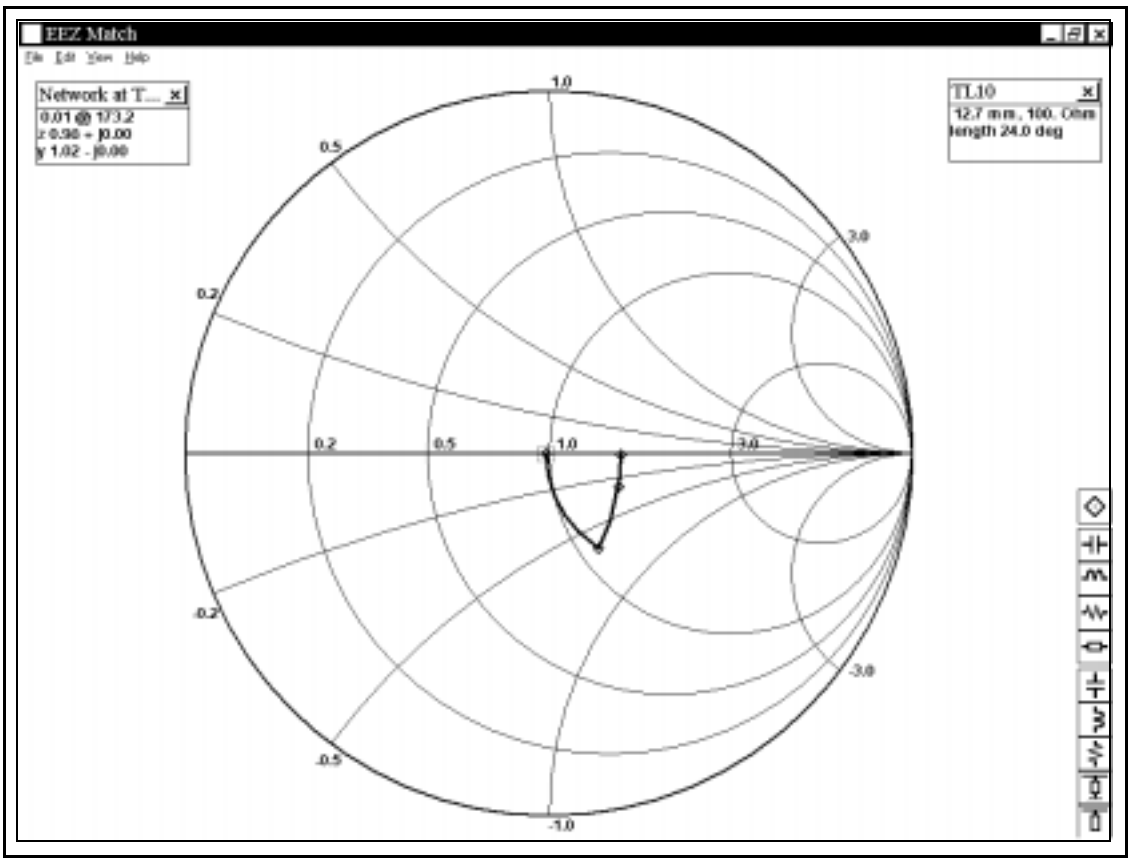


Figure 8 Smith Chart Plot of LNA2OUT Matching Network

EEZ Match Network:

CKT

CAP 6 0 C = 0.25 C11 C = 0.25 pF (Modelled pin stray capacitance)

TLOC 15 0 Z = 35.0 E = 10.18 F = 1.575 (Length E = 10.2 Degrees)

TLIN 6 10 Z = 100.0 E = 24.0 F = 1.575 (Length E = 24 Degrees)

In this network the line width is chosen at 4 mils to provide a characteristic impedance of 100 Ohms. In the network above the line length was chosen at 24 degrees.

Taking the velocity factor calculated above can determine the physical lengths of these lines as follows:

Open Stub at LNA2OUT (Z ~ 35R)

This was used to more accurately model the fractional capacitance required for successful matching of this port.

Electrical lengths of 10 Degrees, Velocity Factor = 3772,

L10 Deg = 10/3772 = 2.65 mm or 104 mils (3.1 mm actually implemented).

Microstrip Line (Z ~ 100R)

Electrical lengths of 24 Degrees, Velocity Factor = 3378,

L24 Deg = 24/3378 = 7.1 mm or 279 mils (7.1 mm actually implemented)

For explanation of differences between the calculated results, and those implemented on the board, (see note Section 3.2.1.2 on Page 26).

IMPORTANT

If a physical shunt capacitor was used on the LNA2 output it would be significantly less than 1 pF. This very small capacitance is very difficult to realise with physical components so on the reference design an open stub microstrip line has been implemented. A via is placed directly at the LNA2OUT pin through to an open ended strip of copper on the other side of the board. This strip of copper is referred to as an open stub. The stub chosen on the reference board realised a 35 Ohm track impedance of length 121 mils.

3.2.5 Mixer1 Input Matching Circuit

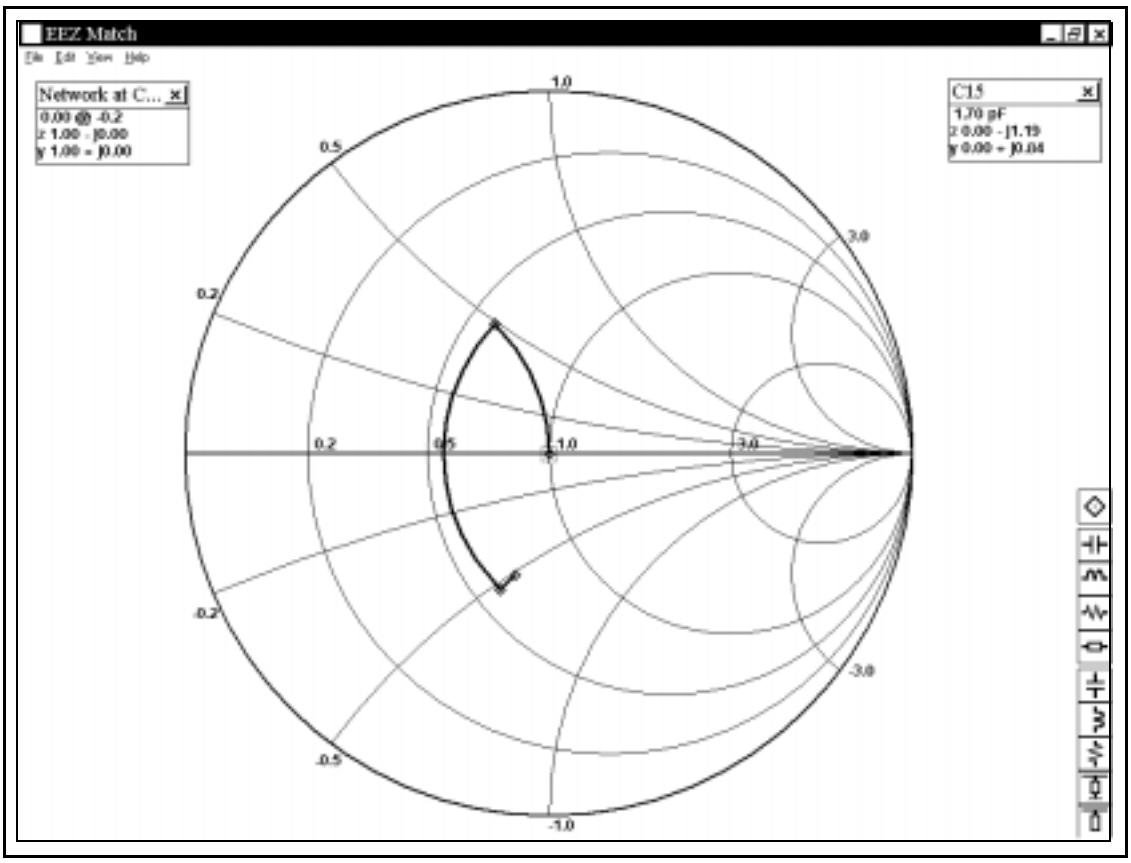


Figure 9 Smith Chart Plot of MIXER1 Input Matching Network

EEZ Match Network.

CKT

CAP 6 0 C = 0.25 ! C13 C = 0.25 pF (Modelled pin stray capacitance)

TLIN 6 11 Z = 100.0 E = 31.0 F = 1.575 (Length E = 31 Degrees)

CAP 11 0 C = 1.7 ! C14 C = 1.7 pF

In this network the line width is chosen at 4 mils to provide a characteristic impedance of 100 Ohms. In the network above the line length was chosen at 31 degrees.

Taking the velocity factor calculated above can determine the physical lengths of these lines as follows:

Microstrip Line (Z ~ 100R)

Electrical lengths of 31 Degrees, Velocity Factor = 3378,

L31 Deg = 31/3378 = 9.2 mm or 362 mils (9.5 mm actually implemented)

For explanation of differences between the calculated results, and those implemented on the board, (see note Section 3.2.1.2 on Page 26).

3.2.6 LNA1 Input Matching Circuit

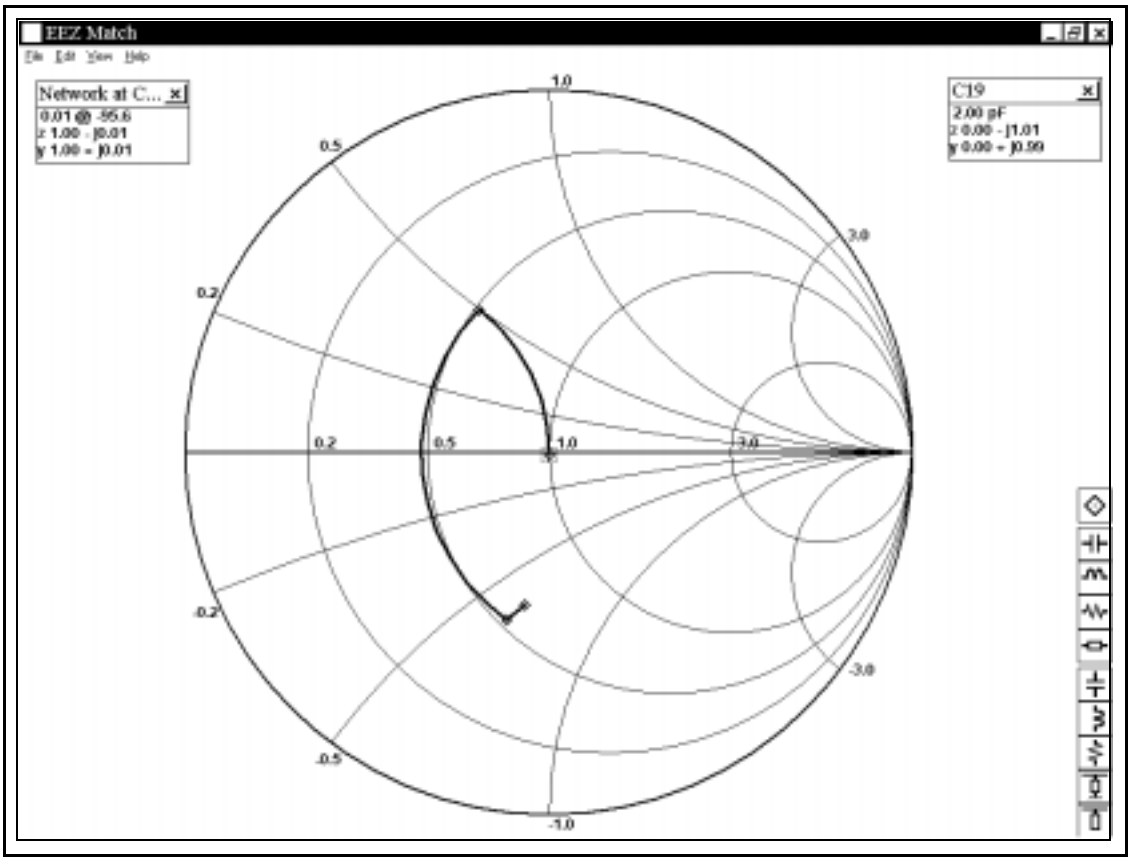


Figure 10 Smith Chart Plot of LNA1IN Matching Network

EEZ Match Network.

CKT

CAP 1 0 C = 0.25 ! C1 C = 0.25F (Modelled pin stray capacitance)

TLIN 1 2 Z = 100.0 E = 33.5 F = 1.575 (Length E = 34 Degrees)

CAP 2 0 C = 2.0 ! C2 C = 2 pF

In this network the line width is chosen at 4 mils to provide a characteristic impedance of 100 Ohms. In the network above the line length was chosen at 34 degrees.

Taking the velocity factor calculated above can determine the physical lengths of these lines as follows;

Microstrip Line (Z ~ 100R)

Electrical lengths of 34 Degrees, Velocity Factor = 3378,

L34 Deg = 34/3378 = 10 mm or 394 mils.

For explanation of differences between the calculated results, and those implemented on the board, (see note Section 3.2.1.2 on Page 26).

3.2.7 LNA1 Output Matching Circuit

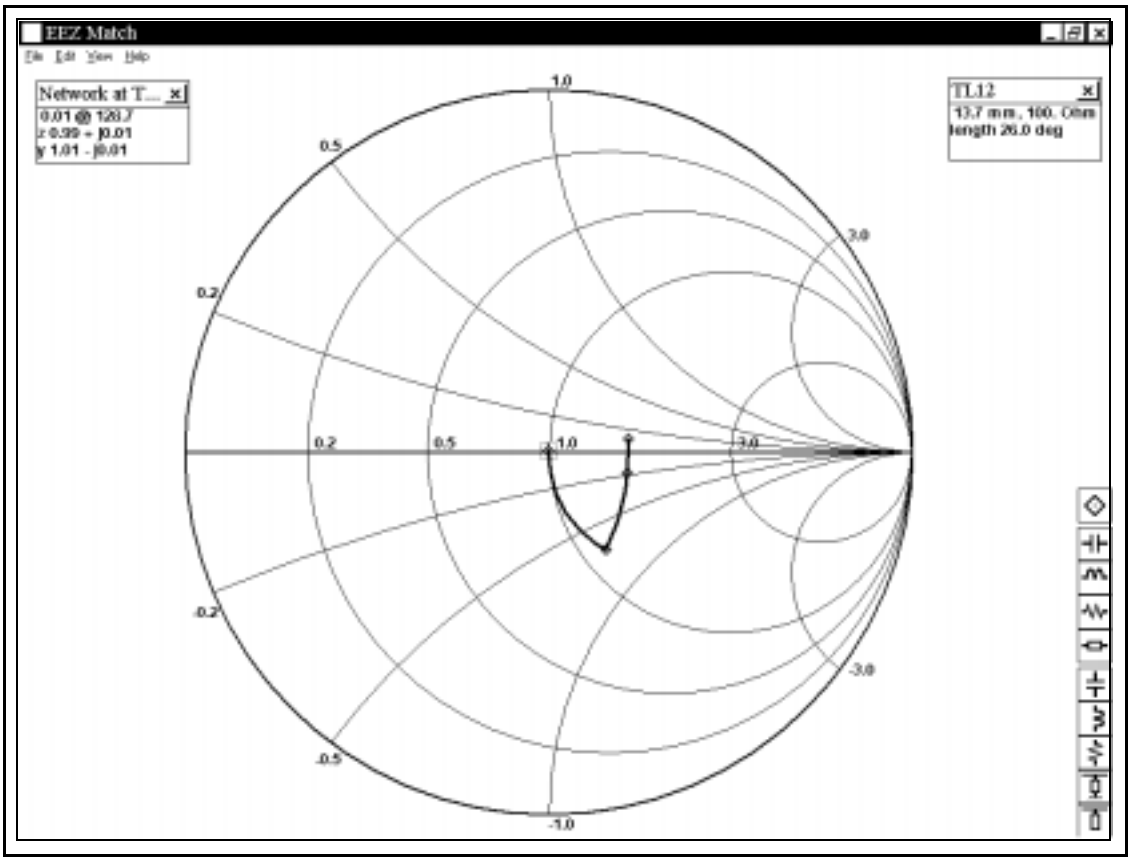


Figure 11 Smith Chart Plot of LNA1OUT Matching Network

EEZ Match Network.

CKT

CAP 1 0 C = 0.25 ! C3 C = 0.25 pF (Modelled pin stray capacitance)

CAP 15 0 C = 6.1886448e-1 ! C10 C = 6.2 pF

TLIN 4 5 Z = 100.0 E = 26.0 F = 1.575 (Length E = 26 Degrees).

In this network the line width is chosen at 4 mils to provide a characteristic impedance of 100 Ohms. In the network above the line length was chosen at 26 degrees.

Taking the velocity factor calculated above can determine the physical lengths of these lines as follows;

Microstrip Line (Z ~ 100R)

Electrical lengths of 26 Degrees, Velocity Factor = 3378,

L26 Deg = 26/3378 = 7.7 mm or 303 mils.

For explanation of differences between the calculated results, and those implemented on the board, (see note Section 3.2.1.2 on Page 26).

3.2.8 Bandpass Filter Selection

There are a vast array of both ceramic bandpass filters and SAW filters specifically designed for the GPS frequency at 1.57542 GHz. On the reference design footprints for both types were implemented for demonstration purposes. On a final board design only one device type should be used and the grounding optimised for this device. Grounding is a particularly important issue with ceramics. If the casing is not adequately grounded then high insertion loss will result which will significantly degrade performance. To this end it is recommended that where possible vias are provided to the inner layer ground planes around the filters and each of the matching network shunt capacitors. This is preferred practice and greatly improves the ground return for this high frequency path.

The Mitsubishi SAW filter was a small part but up to three times the cost of some ceramic parts. The key benefits are size, the improved out of band rejection characteristics and the slightly lower insertion loss. The Murata ceramic filter was very low cost and although not as good as the SAW filter in some respects produced very good results in the final design. The only issue here may be if good out of band rejection is required for frequencies close to the GPS carrier at 1.575 GHz. In this particular case a SAW filter may provide a better solution. Table 12, highlights the general specification for both parts.

Table 12 Bandpass Filter Data for Mitsubishi and MuRata Components

Parameter	Mitsubishi MF1012S-1	MuRata DFC21R57P002HHC
Centre Frequency	1.57542 GHz	1.57542 GHz
Bandwidth	± 1 MHz	± 1 MHz
Insertion Loss at BW	2.7 dB	3.5 dB
Ripple at BW	1.0 dB	0.5 dB
VSWR at BW	2.0 dB	2.0 dB
Stopband Attenuation	30 dB minimum @ 50 MHz	15 dB minimum @ 50 MHz

3.3 VCO and PLL Filter

The VCO is tuned by a varactor and Inductor network to provide a local oscillator at around 1.5336 GHz. The varactor chosen on the reference design exhibits a typical total Ct at 1 V of 1.5 pF. Once the effects of the 15 pF series capacitor, SFR effects of the inductor and all stray effects are accounted for we have a nominal effect capacitance of 2.3 pF. This means an inductor in the order of 4.7 nH is required to provide the desired VCO frequency as shown:

$$F = 1/(2\pi\sqrt{LC}) = 1/6.52\times10^{-10} = 1.5336\text{GHz}$$

Where C = 2.3 pF and L = 4.68 nH

The LC network tunes the VCO to the desired frequency whilst the loop filter components provide bandpass filtering to eliminate high frequency interference and optimize phase noise response. The use of 0805 air core inductors such as the coilcraft 0805CS range will yield the highest effect Q and ultimately best wideband phase noise performance. In order to maintain optimal phase noise performance it is essential that VCO ground and supply inductances are minimal. This requires close proximity layout with ground returns directly to IC pins and also a liberal use of ground vias where practical. If stray inductance problems occur it will become obvious through the need to implement lower values of physical inductor for the VCO circuit. The reference design uses a 5.6 nH inductor. Values much less than this, ie: 3.9 nH suggest improvements in layout are required.

3.3.1 VCO

This section details the function of the VCO circuit and the purpose of each section.

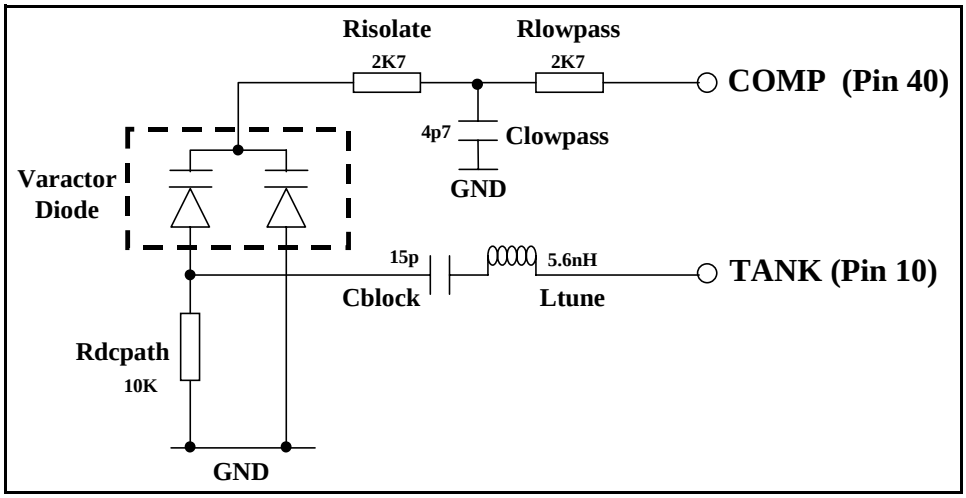


Figure 12 Typical VCO Circuit Configuration

The comparator output pin of the UAA1570 provides the DC control to tune the varactor diode for the implemented inductor. The operating range of the COMP output is between 0 V and Vcc - 0.6 V. Therefore in a 3 V system we need to set the nominal tuning voltage midway between 0 and 2.4 V, ie: 1.2 V. By doing this we provide the maximum tuning range for the application to take into account component tolerances in production.

1) Rlowpass and Clowpass provide filtering to attenuate higher frequency harmonics of the reference oscillator. The -3 dB cut off of this filter is nominally set just below the reference clock frequency, and in this case 12.5 MHz.

2) Risolate provides isolation from the varactor circuit. This prevents Clowpass from greatly detuning the VCO.

3) The varactor chosen primarily for minimum capacitance at nominal tuning voltage of 1 V. The smaller the diode capacitance Ct, the higher the inductor value that can be used, which makes tolerance effects and layout less critical. Another factor is series resistance, where the higher the resistance the better the Q factor.

4) Rdcpath is used to provide a DC path for the tuning, as in this application a varactor pair has been used in series to minimise overall capacitance.

5) Cblock and Ltune complete the tuning circuit. Cblock provides the AC coupling and is chosen for low impedance at the VCO frequency. This ensures the tuning is controlled only by the varactor and inductor, Ltune.Cblock can also be used to pull the resonator circuit and required inductance to more practical values whilst optimising DC tuning centering.

It is possible to use a single varactor in which case the anode would be tied to GND with the cathode tied to the junction of Risolate and Cblock. The main reason for not doing this was to ensure reasonably high inductor values could be realised.Another key reason for using double series varactor diodes was to maximise the VCO gain, Ko, by minimising series varactor capacitance at the negative input VCO TANK pin. Therefore using double series varactor diodes such as the SMV1233-004 maximises the realisable inductor values, VCO gain and resonator Q.

Circuit parasitics inevitably mean that the overall Q of the resonant circuit is not very high. However an 0805 inductor will make a significant difference to out of band phase noise, compared to an 0603 part. To this end it is strongly recommended that 0805 inductors with high Q are used in the final solution, such as the Coilcraft 0805CS range.

3.3.2 Phase Locked Loop Filter

The purpose of the loop filter is to set the operating bandwidth of the VCO and optimize phase noise through outband attenuation.

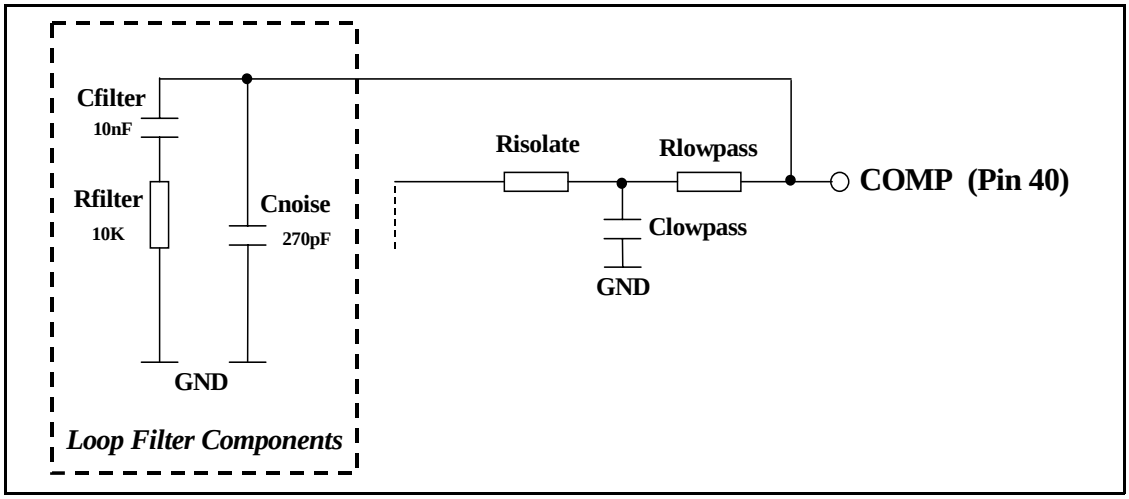


Figure 13 VCO Loop Filter Circuit

The loop filter bandwidth is set typically around 35 kHz or less. The following equations can be used to provide an estimate of component values for given loop bandwidths.

Table 13 Constants Required for VCO Loop Filter Calculation

Label	Value	Comments
F(bw)	35 kHz	Loop filter bandwidth being designed for (Nominally 35 kHz)
k	2.2	Damping coefficient. (nominally 2 to 3 to minimise side lobe peaks either side of the VCO spectrum
Kp	290 µA	Maximum charge pump current (Icp maximum from data sheet). It is expected that this never goes above 290 µA
Ko	75M Hz/V	VCO gain typically between 60 MHz/V and 100 MHz/V so in this case chosen as nominally 75 MHz/V
N	852	Divide ratio of VCO operating frequency and phase comparator frequency. The VCO runs at 1.5336 GHz and the phase comparator operates at 1.8 MHz, hence 852

Firstly Calculating Wo:

Calculating for Cfilter:

$$Cfilter = (Kp \times Ko)/(Wo^2 \times N) = 10.77nF$$

$$Wo = 2\pi F(bw) / \left(\sqrt{1 + 2(k)^2 + \sqrt{(1 + 2(k)^2)^2 + 1}} \right) = 48675$$

Calculating for Rfilter:

$$Rfilter = (2 \times k) / (Wo \times Cfilter) = 8.39K$$

Cnoise provides filtering of the high frequency harmonics of the reference and sample clocks. This is nominally chosen at around 30 or 40 times lower than Cfilter. In the reference design Cnoise was chosen at 270 pF, approximately 40 times lower than Cfilter. If this is made too high in relation to Cfilter it can start to affect the damping which could be identified by increase in the side lobe peaks of the VCO spectrum.

Once the nominal values for the loop filter are calculated the resulting response can be measured at the bench and altered slightly to provide the desired characteristics. In the case of the reference design a 10 NF and 10 k combination was implemented.

3.4 First IF Filter

The first IF filter performs four key functions:

- Selectivity to protect second mixer from spurious RF signals passing through RF Filter(s).
- Attenuates thermal noise and 2nd mixer image frequency.
- Impedance transformation from RF mixer output to the IF2 mixer input.
- If a double ended structure is implemented, it can enable better common mode rejection of spurious high level sources which have externally coupled into the filter path, such as the 3rd harmonic of the reference clock.

For the Philips Reference Design a 6th order, coupled resonator filter based on a Butterworth response has been implemented. This section details the filter design used on the reference board, but section 3.6, describes how a dedicated SAW filter could be implemented into the design as a replacement.

There were two critical aspects to the design to the design of the first IF filter,

- Minimum bandwidth of 2 MHz + headroom to account for component tolerances.
- Rejection of 2nd mixer image frequency at 34.86 MHz (At least 13 dB).

The filter design was then determined using the capacitively coupled resonator approach based on 3 dB down k and q values from a 3rd order Butterworth lowpass response. This procedure is detailed in the Handbook of Filter Synthesis by Anatol I Zverev Reference [4]. This was originally chosen for its simplicity as well as selectivity advantage versus component count.

3.4.1 Filter Specification

The first IF filter was chosen with the following characteristics:

Centre Frequency	41.82 MHz
3 dB Bandwidth	5 MHz
Outband Attenuation	> 13 dB at 34.86 MHz.

To achieve the required attenuation characteristics a 3rd order filter was opted for. Graphs are provided in Reference [4] which make the order of the filter easy to decide upon.

3.4.2 IF1 Filter Design Procedure

First the inductive or capacitive element is chosen such that it will yield realisable values for the final filter design keeping in mind that the filter is being driven from a transconductance mixer output. That is the conversion gain of the mixer and delivered output power are maximised by maximising the real impedance level in an I^2R relationship. Since the filter design impedance levels are proportional to the inductance as R = Q x Wo x L, we would like to maximise the reference inductance level. A balance has to drawn to ensure at the same time that the associated tank and coupling capacitances tolerances do not become impractically small.

Generally, coupled resonator filters design input and output impedance are not realised exactly due to the availability of discrete component value. Care should be taken to calculate the realised impedance of the actual filter to detect and adjust significant divergence from the initial design impedance objective at both the input and output of the filter.

To realise the tabular response and insertion loss, the filter must be driven from and terminated in the design impedance. Care must be taken to ensure that the Q effects of the input and output tank inductors are taken into account in determining this loading. That is the finite Q's of the tank inductors should be considered as providing an appropriate portion of these required source and load impedances.

In this case the inductor was chosen at 165 nH. This should then provide capacitive values in the order of 90 pF for each resonator section, given the equation below:

$$Fo = 1/(2\pi\sqrt{LC})$$

Therefore with Fo at 41.82 MHz and L = 165 nH, C would be 88 pF. The 165 nH in would yield a typical Q factor in the order of 40 for most practical components. This now enables us to calculate the value of qo which will determine what k and q values to implement from the filter tables in Reference [4].

$$qo = BW_{3dB} \times Q/(Fo) = 5 \times 40/41.82 = 4.78$$

Using qo = 5 we can now extract the following values from the design tables. Tables are provided in Reference [4], which allow the k and q values to be extracted based upon a typical loaded Q factor for the resonators.

qo = 5, q1 = 0.8226, qn = 1.7115

k 12 = 0.6567, k 23 = 0.7060

insertion Loss = 4.742

Having now determined the table constants for a 3rd order Butterworth filter and also chosen resonator components L and C we can now calculate the full circuit values.

Having chosen L at 165 nH and therefore C at 88 pF the following can be calculated, where the series

$$C12 = (k12 \times BW3dB \times C)/(Fo) = 6.9pF$$

capacitors, C12 and C23 provide the capacitive coupling between the tank nodes and the shunt capacitors, Ca, Cb and Cc are the physical nodal capacitances which provide the specified total capacitance of 88 pF in conjunction with the coupling capacitors.

$$Ca = C - C12 = 81.1pF$$

Continuing on we can now calculate all the remaining capacitive elements.

$$C23 = (k23 \times BW3dB \times C)/(Fo) = 7.4pF$$

$$Cb = C - C12 - C23 = 73.7pF$$

$$Cc = C - C23 = 80.6pF$$

We can now determine the load and source impedances that will ensure the desired response is obtained. Firstly we need to denormalise the tabular values for q1 and qn to determine the estimated Q factor of the filter source and load, as shown below:

$$Q_{denormalise} = (Fo)/(BW3dB) = 8.361$$

$$Qs = Q_{denormalise} \times q1 = 8.361 \times 0.8226 = 6.88$$

The denormalised Q factor for the filter load can be determined in the same way, in this case yielding a value of 14.31, where qn = 1.7115.1

$$Rs = Qs \times 2\pi Fo \times L$$

Therefore when inserting values for Q_S and Q_L in the equation above, given L = 165 nH, the following source and load impedance for the filter can be determined.

R_S = 298 Ohms, and R_L = 620 Ohms.

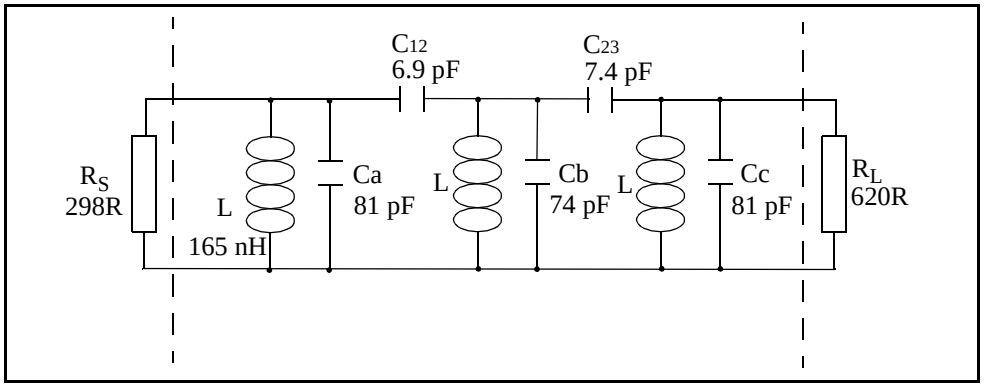


Figure 14 Single-Ended 6th Order IF1 Filter Design (Based on 3rd Order Butterworth Lowpass)

At this stage we have a complete filter design that if simulated in SPICE or other simulation program would provide the required filter response. Inevitably the values that result are never practical and so it is necessary to select preferred component values by trial and error simulation and verification on the PCB itself. In our case we have chosen the first IF stage to be double ended to provide common mode rejection of the 14.4 MHz reference clock harmonics. In order to convert this structure into a double ended design we simply superimpose an identical network over the current one such that the shunt elements connect in series. In simple terms the shunt inductors and resistors are doubled and the capacitances halved. The series coupling capacitors remain unchanged. The single ended structure is shown in Figure 14 and the converted structure is shown in Figure 15. The SPICE netlist for this filter is provided in Appendix A.

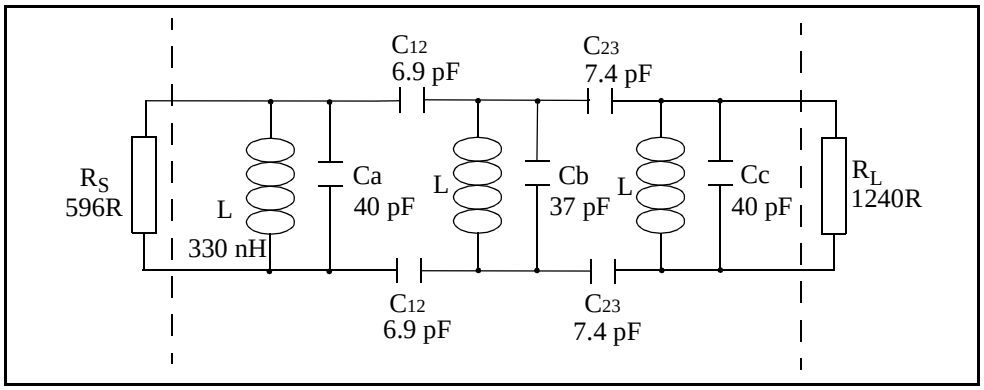


Figure 15 Double-Ended 6th Order IF1 Filter Design (Based on 3rd Order Butterworth Lowpass)

In practice we want to maximise the real inband loading of the transconductance mixer output. The tabular filter component values, R_S and R_L result in the prescribed filter response, but do not guarantee the inband impedances seen at the input or output of the filter. These must be determined by calculation over the frequency band with the actual component values used in the implemented design. Small changes in the selected values can result in significant inband impedance ripple and unexpected results.

After calculating or simulating the realised filter input and output impedance against the associated filter response expectation, you may want to reverse the input and output ports, as we have done, to present the highest in band impedance to the first mixer output. This is to maximise gain and stability, while minimising post filtering stray spurious pick-up, by presenting the lowest port impedance of the filter to the input of the second mixer.

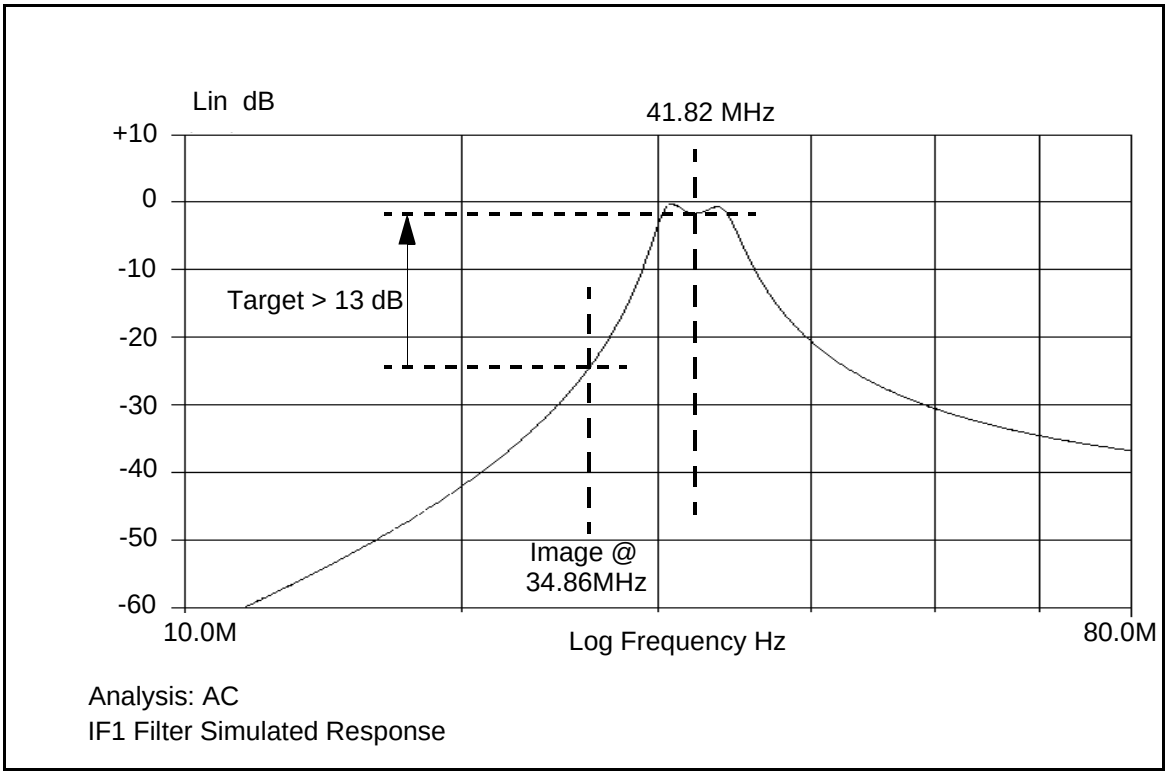


Figure 16 Simulated Response of IF1 Filter at 41.82 MHz

Note in both cases RS and RL are not physical components rather the required load to ensure the specified filter response is achieved and so the loads presented to the filter input and output must be determined. The load RL is calculated from the equivalent Q loss resistance of the inductor in parallel with a physical resistor. In order to maintain filter characteristics, as indicated in Figure 16, we need to tune this parallel combination to provide an effective load close to 1240R.

Firstly calculate the series equivalent Q loss resistance of the inductor. After detailed simulation and calculation the final total inductance at the mixer1 output was made up of two separate components of 180 nH, providing a total effective shunt inductance of 360nH. The total inductance was split in order to allow both mixer outputs to be DC biased through the inductive elements of the filter.

$$r = 2 \times \pi \times Fo \times L / Q = 2.365 Ohms$$

In this instance the unloaded Q factor of the inductors could be expected to be in the order of 40, with Fo at 41.82 MHz. Therefore in this case r = 2.365 Ohms. We can now determine the inductor equivalent load as follows:

$$Req = r \times Q^2 = 3783.8 Ohms$$

We need to present a physical load resistor at the output of Mixer1 to reduce the effective load close to 1240 Ohms. Given Req = 3784 Ohms we can determine the approximate required R to complete the filter input load.

$$Rload = Req \times R/(Req + R) = (3784R)/(3784 + R) = 1240$$

$$R = 4692160/2544 = 1844Ohms$$

Therefore in theory only a 1.8 k Ohm resistor should be required in parallel with the filter input to maintain the desired filter response. The final value chosen on the reference design was somewhat higher at 12 k, and was chosen based on detailed simulation and test results. In practice the filter impedance was lower than anticipated and so a compromise was made between maximising the conversion gain of the mixer whilst maintaining the desired filter response.

The output of the filter is then completed in a similar way except in this instance the Mixer2 differential input resistance of 2.05 k Ohms must also be considered. Therefore if Req = 3784 Ohms and the Mixer2 input = 2.05 k Ohms the existing load is already at 1308 Ohms, (ie: 3.78 k // 2.05 k. In order to provide an equivalent load of 596 Ohms a load resistor of 1095 Ohms is required. Again after selecting preferred values of L and C a shunt resistor of 909 Ohms was eventually chosen to provide the desired filter response.

The theory on the filter design given in this section details the approach and provides an approximation to the required solution. In practice the values inevitably need to be altered to find preferred equivalents and it is therefore partly an exercise of trial and error to achieve the realisable result. As stated earlier in this section once the filter is designed detailed calculations and/or simulations need to be carried out to carefully determine the realisable filter characteristics in a real application. From the schematics in Section 6.1 on Page 76 it can be seen that in practice the final filter design differs slightly from that produced in the initial design process.

3.4.3 Verifying Maximum First Mixer Output Voltage Swing

The first mixer output voltage swing must be limited to 1 V peak differential in order to prevent clipping of the output ESD protection diodes. Under normal operating conditions the satellite signal level is so low that clipping at the mixer1 output is extremely unlikely. The main issue here is the maximum expected in-band jammer level and its effect on the mixer compression points. In theory a 1-Bit system such as EXACT with a good system Noise Figure cannot handle more than a 35 dB J/S ratio at the input of the 1-Bit quantizer, regardless of satellite level. It is important to verify at this stage that under worst case allowable jamming conditions that the mixer is not placed into compression and that clipping at the mixer output is also avoided. In order to verify performance under these conditions it is important to accurately determine the realised loads seen at both the mixer input and output. The actual loads presented at both the input and output of the first mixer are given in Table 15 on Page 49 and are based on detailed simulations. Given the information in Table 14 on Page 43, we can determine that the nominal expected mixer input level will be -78 dBm, under typical operating conditions.

.

Table 14 Gain Stages Prior to Mixer1 input

Symbol	Gain	Comments
Sat Level	-117 dBm	The maximum likely GPS satellite signal level at antenna (-120 dBm maximum specified output + 3 dB to allow for sats running hot)
Antenna	26 dB	Maximum Active Antenna Gain including cable losses
LNA2	13 dB	Typical LNA2 gain including Bandpass Filter Loss
Maximum J/S	35 dB	Maximum Jammer to Signal Ratio

$$\mathrm{Mixer1Input} = -117\mathrm{dBm} + 26\mathrm{dB} + 13 = -78\mathrm{dBm}$$

This gives 53 dB headroom on the -1 dB compression point of the first mixer, typically -25 dBm, and more than accounts for the maximum allowable jammer to signal level of 35 dB.

Symbol	Value	Description
CP	-43 dBm	Nominal mixer input with 35 dB J/S ratio
R	50 Ohms	Matched Input Impedance of Mixer1
Zout	860 Ohms	Effective load presented at Mixer1 output
Zin	630 Ohms	Effective load presented at Mixer2 input
Y21	0.0531 A/V	Typical Conversion Transconductance at 3 V
IF1 Out	1 V peak	Maximum differential Mixer1 output swing (ie: 2 V p - p)

Having verfied this it is now important to confirm that under these worst case jamming conditions the output of the mixer is not clipped. Using the values provided in Table 15 on Page 49 we can determine the typical mixer output level and the maximum load that can be presented to avoid clipping at the output, under these conditions. With an in band jammer to signal level of 35 dB the maximum input to the first mixer would be -43 dBm.

$$\mathrm{Mixer1Input} = -117\mathrm{dBm} + 35\mathrm{dB} + 26\mathrm{dB} + 13 = -43\mathrm{dBm}$$

Converting -43 dBm to peak voltage;

$$\mathrm{Vp} = \sqrt{0.001 \times 10^{\mathrm{CP}/10} \times 2 \times \mathrm{R}} = \sqrt{5 \times 10^{-6}} = 2.24\mathrm{mVPeak}$$

Given the conversion transconductance of the mixer and the effective load at the output from Table 15 on Page 49 the differential output voltage, Vout, can be calculated as:

$$\mathrm{Vout} = 2.24\mathrm{mV} \times 0.0531 \times 860 = 0.102\mathrm{VPeak}$$

This is well within the recommended limit of 1 V peak differential. It can be further shown that if the mixer was driven to its -1 dB compression point of typically -25.4 dBm, or 17.8 mV Peak, that the corresponding output still remains less than the 1 V peak recommended limit.

$$Vout = 17.8mV \times 0.0531 \times 860 = 0.813VPeak$$

This means that even if the mixer was driven to compression at the input the corresponding output would still be low enough to avoid potential clipping of the ESD protection diodes.

3.5 Second IF Filter

For the Philips Reference Design a 6th order, coupled resonator filter based on a Butterworth response has been implemented.

There were three critical aspects to the design to the design of the first IF filter:

- Bandwidth of nominally 2 MHz
- Filter impedance levels required to maintain stability around the quantizer loop
- Providing anti-alias selectivity for the sampling rate and sample mixed second IF of 1.32 MHz, (default application), actually used in the DSP baseband processing.

The noise bandwidth of the GPS system is predominantly determined by the noise bandwidth of the second IF filter. A somewhat wider than necessary C/A code bandwidth was used here to accommodate component tolerances.

Since the filter impedance was chosen low enough to ensure that signal coupling from the SIGN bit output back to the quantizer input, or IF2 filter output, a single ended design was implemented to save components. Also normal spurious products were not considered a significant problem in the second IF.

Using a 6th order Butterworth bandpass design provides improved alias attenuation between the sampled passbands at the adjacent alias overlap point in the resulting spectrum. A somewhat wider than necessary C/A code bandwidth was used here also to accommodate component tolerances.

The filter design was determined using the capacitively coupled resonator approach based on 3 dB down k and q values for a 3rd order Butterworth response. This procedure is detailed in the Handbook of Filter Synthesis by Anatol I Zverev Reference [4]. This was originally chosen for its simplicity as well as selectivity advantage versus component count.

3.5.1 Filter Specification

The second IF filter was chosen with the following characteristics:

Centre Frequency	3 MHz

(Actually 3.48 MHz but chosen lower to compensate for geometric asymmetry given low frequency)

3 dB Bandwidth	1.75 MHz

(In practice Q loss will result in higher bandwidth in practice, ie greater than 2 MHz)

To maintain good outband attenuation characteristics a 3rd order filter was opted for. Graphs are provided in Reference [4] which make the order of the filter easy to decide upon.

3.5.2 IF2 Filter Design Procedure

First the inductive or capacitive element is chosen such that it will yield realisable values for the final filter design keeping in mind that the filter is being driven from a transconductance mixer output. That is the conversion gain of the mixer and delivered output power are maximised by maximising the resistive port impedance level in an I^2R relationship. Since the filter design impedance levels are proportional to the inductance as R = Q x Wo x L, we would like to maximise the reference inductance level. A balance has to be drawn to ensure at the same time that the associated tank and coupling capacitances tolerances do not become impractically small.

Generally, coupled resonator filters design input and output impedance are not realised exactly due to the availability of discrete component values. Care should be taken to calculate the realised impedance of the actual filter to detect and adjust significant divergence from the initial design impedance objective at both the input and output of the filter. To realise the tabular response and insertion loss, the filter must be driven from and terminated in the design impedance. Care must be taken to ensure that the Q effects of the input and output tank inductors are taken into account in determining this loading. That is the finite Q's of the tank inductors should be considered as providing an appropriate portion of these required source and load impedances.

First the inductive or capacitive element is chosen such that it will yield realisable values for the final filter design. In this case the inductor was chosen at 22 μH. This should then provide capacitive values in the order of 128 pF for each resonator section.

$$Fo = 1/(2\pi\sqrt{LC})$$

Therefore given the equation above with Fo at 3 MHz and L = 22 μH, C would be 128 pF. The 22 μH in many practical cases would yield a typical Q factor in the order of 40. This now enables us to calculate the value of qo which will determine what k and q values to implement from the filter tables in Reference [4].

$$qo = BW_{3dB} \times Q/(Fo) = 1.75 \times 40/3 = 23.33$$

Using qo = 20, as the closest match, we can now extract the following values from the design tables. Tables are provided in Reference [4], which allow the k and q values to be extracted based upon a typical loaded Q factor for the resonators.

qo = 20, q1 = 0.8041, qn = 1.4156

k 12 = 0.7687, k 23 = 0.6582

Insertion Loss = 0.958

Having now determined the table constants for a 3rd order Butterworth filter and also chosen resonator components L and C we can now calculate the full circuit values.

Having chosen L at 22 µH and therefore C at 128 pF the following can be calculated, where the series capacitors, C12 and C23 provide the capacitive coupling between the tank nodes and the shunt capacitors, Ca, Cb and Cc are the physical nodal capacitances which provide the specified total capacitance of 128 pF in conjunction with the coupling capacitors.

$$C12 = (k12 \times BW3dB \times C)/(Fo) = 57.4pF$$

.

$$Ca = C - C12 = 70.6pF$$

Continuing on we can now calculate all the remaining capacitive elements.

$$C23 = (k23 \times BW3dB \times C)/(Fo) = 49.1pF$$

$$Cb = C - C12 - C23 = 21.5pF$$

$$Cc = C - C23 = 78.9pF$$

We can now determine the load and source impedances that will ensure the desired response is obtained. Firstly we need to denormalise the tabular values for q1 and qn to determine the estimated Q factor of the filter source and load, as shown below:

$$Q_{denormalise} = Fo/BW3dB = 3/1.75 = 1.715$$

$$Qs = Q_{denormalise} \times q_1 = 1.38$$

The equation above calculates the denormalised Q factor for the filter source, but the denormalised Q factor fo the filter load can be determined in the same way, in this case yielding a value of 14.31, where qn = 1.7115.1.

$$Rs = Qs \times 2\pi Fo \times L$$

Therefore when inserting values for Q_S and Q_L in the equation above, given L = 22 µH, the following source and load impedance for the filter can be determined.

R_S = 572 Ohms, and R_L = 1008 Ohms.

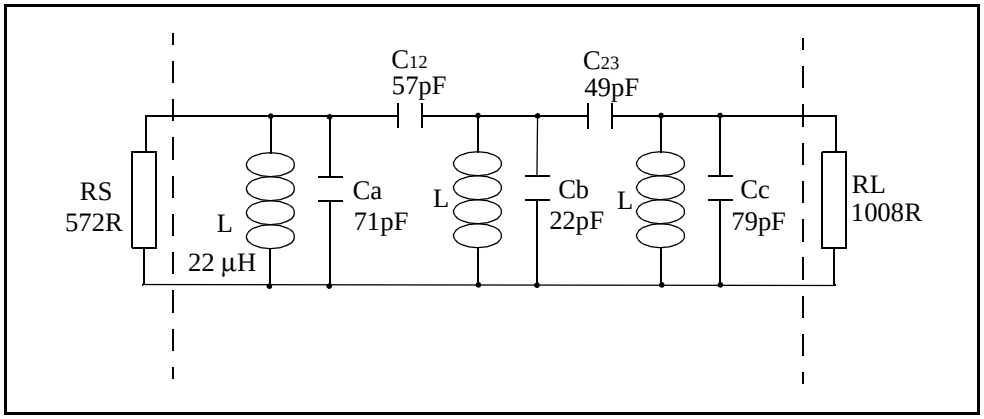


Figure 17 Single-Ended 6th Order IF2 Filter Design (Based on 3rd Order Butterworth Lowpass)

At this stage we have a complete filter design that if simulated in SPICE or other simulation program would provide the required filter response. Inevitably the values that result are never practical and so it is necessary to select preferred component values by trial and error simulation and verification on the PCB itself. In this design the second IF filter was kept single ended to minimise cost.

In practice we want to maximise the real inband loading of the transconductance mixer output. The tabular filter component values, R_S and R_L result in the prescribed filter response, but do not guarantee the inband impedances seen at the input or output of the filter. These must be determined by calculation over the frequency band with the actual component values used in the implemented design. Small changes in the selected values can result in significant inband impedance ripple and unexpected results. The SPICE netlist for this filter is provided in Appendix B.

After calculating or simulating the realised filter input and output impedance against the associated filter response expectation, you may want to reverse the input and output ports, as we have done, to present the highest in band impedance to the first mixer output. This is to maximise gain and stability, while minimising post filtering stray spurious pick-up, by presenting the lowest port impedance of the filter to the input of the Limiter.

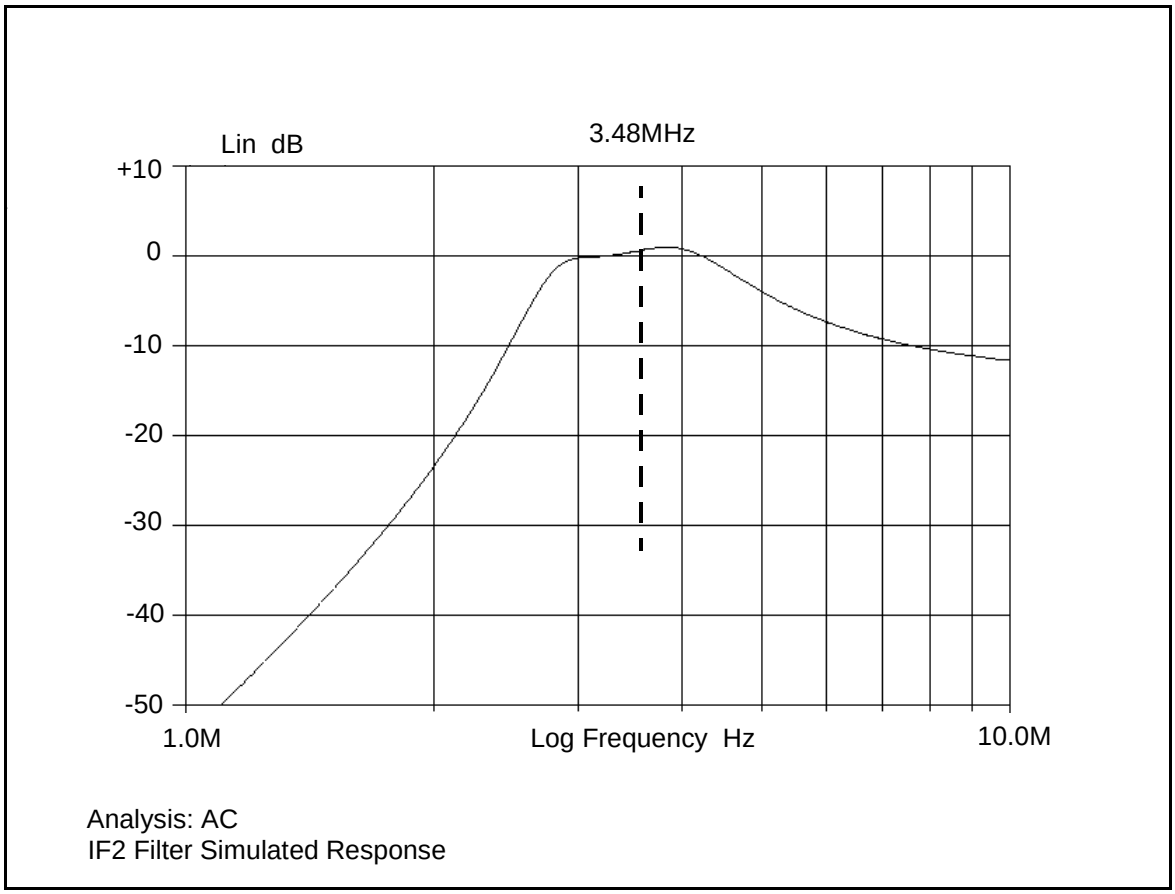


Figure 18 Simulated Response of IF2 Filter at 3.48 MHz

Note in both cases RS and RL are not physical components rather the required load to ensure the specified filter response is achieved. The load presented to the filter input and output must be determined. The load RL is calculated from the equivalent Q loss resistance of the inductor in parallel with a physical resistor. In order to maintain filter characteristics, as indicated in Figure 18, we need to tune this parallel combination to provide an effective load close to 1008R.

Firstly calculate the series equivalent Q loss resistance of the inductor; Note in this case that the final filter design used a 27 μH inductor as opposed to 22 μH used in the initial design process. Again this was a result of detailed simulations taking into account loss effects encountered in a real design.

$$r = 2 \times \pi \times Fo \times L / Q = 14.76 Ohms$$

In this instance the Q of the inductors could be expected to be in the order of 40, with Fo at 3.48 MHz. Therefore in this case r = 14.76 Ohms. We can now determine the inductor equivalent load as follows:

$$Req = r \times Q^2 = 23.615 KOhms$$

Therefore we need to present a physical load resistor at the output of Mixer2 to reduce the effective load close to 1008 Ohms. Given Req = 23.6 K Ohms we can determine the approximate required R to complete the filter input load.

$$Rload = Req \times R/(Req + R) = (23615R)/(23615 + R) = 1008$$

Therefore calculating for R we get:

$$R = 23803920/22607 = 1053Ohms$$

Therefore in theory only a 1 k resistor should be required in parallel with the filter input to maintain desired filter response. In the final application a 2 k resistor was implemented to overcome other losses and maximise the conversion gain of the second mixer.

The output of the filter is then completed in a similar way. Because the inductor equivalent resistance is so high for the 27 µH in this design it is really a case of adding the calculated load directly to the output of the filter. In this case a 572 Ohm resistor was specified but in practice an 820 Ohm was selected. As discussed earlier in this section the final values chosen for the design are likely to differ slightly from the theoretical once all loss effects have been fully taken into account.

3.5.3 Verifying Maximum Second Mixer Output Voltage Swing

As in the case of the first IF design, the main concern is the maximum expected in-band jammer level and its effect on the mixer compression points. In theory a 1-Bit system such as EXACT with a good system Noise Figure cannot handle more than a 35 dB J/S ratio at the input of the 1-Bit quantizer, regardless of satellite level. In the case of the reference design we can establish the likely maximum input to Mixer2 to determine what the maximum permissible load would be before clipping occurs at the output. In this case the design employs an active antenna with a single UAA1570 LNA application. The actual loads presented to the Mixer2 input and output were determined by detailed simulations and are provided in Table 16 on Page 50.

Table 15 Gain Stages Prior to Mixer2 Input

Symbol	Gain	Comments
Sat Level	-117 dBm	The maximum likely GPS satellite signal level at antenna (-130 dBm minimum specified level + 13 dB)
Antenna	26 dB	Total Active Antenna Gain including cable losses
LNA2	13 dB	Typical LNA2 gain including bandpass filter loss
Mixer1	18 dB	Typical Power matched gain of first Mixer
IF1 Loss	-4 dB	Nominal Insertion loss of first IF filter
Maximum J/S	35 dB	Maximum Jammer to Signal Ratio

Given the figures in Table 15. we can estimate the mixer2 input level under normal operating conditions to be -64 dBm.

$$Mixer1Input = -117dBm + 26dB + 13dB + 18dB - 4dB = -64dBm$$

This would result in a peak differential input voltage to the second mixer of 0.65mV Peak, where the load,

$$Vp = \sqrt{0.001 \times 10^{CP/10} \times 2 \times R} = \sqrt{0.502 \times 10^{-6}} = 0.708mVPeak$$

R, is approximated to 630 Ohm. (Effective loading at the Mixer2 input as defined during the design of the first IF filter in Section 3.4.3 on Page 42) Given typical -1 dB compression point for mixer2 o 67.2 mV Peak differential, it can be shown that under normal signal conditions the system would provide approximately 40 dB headroom on the typical compression point of the second mixer.

Table 16 Second Mixer Characteristics

Symbol	Value	Description
-1 dB Point	67.2 mV Peak	Typical -1 dB compression point of Mixer2 (Peak Differential)
Rin	630 Ohms	Effective load impedance seen at Mixer2 input
Rout	825 Ohm	Effective load impedance seen at Mixer2 output
Y21	0.0294 A/V	Typical Conversion Transconductance at 3 V
IF2 Out	0.5 V peak	Maximum single ended Mixer2 output swing

$$Difference = 20\log(0.708/67.2) = -39.5dB$$

If an inband jammer is applied at a J/S ratio of 35 dB, the mixer 2 input level will rise to -29 dBm (Given by -64 dBm + 35 dB). An input of -29 dBm corresponds to a peak differential input voltage of approximately 40 mV, given the input impedance environment of 630 Ohms.

$$Vp = \sqrt{0.001 \times 10^{CP/10} \times 2 \times R} = \sqrt{1.59 \times 10^{-3}} = 39.88mVPeak$$

Given the output impedance and conversion transconductance in Table 16, the corresponding single ended output voltage at mixer2 can be calculated at 0.484V peak, which falls within the recommended limit of 0.5 V peak.

$$Vout = 0.0399 \times (0.0294/2) \times 825 = 0.484VPeak$$

Therefore under worst case allowable jamming conditions it can be verified that in a typical system the mixer2 input does not reach compression and potential clipping at the mixer output is also avoided.

3.6 SAW Filter Implementation for IF1

The use of a SAW filter in the first IF is problematic and requires careful consideration of a number of special issues.

1) Insertion loss of IF SAW filters is typically quite high. Typical insertion losses range from 8 dB to 35 dB for IF frequencies in the range of 30 MHz to 300 MHz. Developing sufficient gain to overcome this loss can be difficult in light of specialized source and load impedance considerations below.

2) Many off-the shelf SAW devices are designed and specified against simple 50 Ohm source and loads. Others require elaborate matching networks. Unfortunately, these specialized termination requirements affect mixer output power, filter insertion loss, response, and group delay.

3) IF SAW filters with 50ns-pp group delay variation (ripple and warping) are suitable for GPS applications. Ripple is used here to describe the intrinsic chatter in an otherwise flat group delay response, while warping refers to larger scale deformations, such as "S" shaping across the entire pass band of the filter. Significant warping of SAW filter group delay response can result if matching is attempted on a filter designed to be unmatched and driven from 50 Ohm source. Likewise, group delay warping can result if a SAW filter, designed to be used with specific matching networks, is driven from arbitrary resistive source/load terminations.

4) Triple-Transit of signals through SAW devices can often result in destructive wave combinations. To avoid this many SAW designs actually expect and require large insertion losses, which are relied upon to attenuate these reflected waves. That is arbitrary power matching could result in unspecified filter response and or increased group delay variations.

5) The designer will generally find a frustrating physical package size trade-off associated with improvements in each performance category.

The specific details and effects of these driving and loading specifications can be difficult to determine. SAW manufacturers must be pressed to provide the information specific to each design. Alternately, a detailed characterization must be undertaken. Consequently, it is very difficult to offer a straight forward standard solution to this problem. However, advice for two categories of SAW filter implementation can be offered. The first category is for simple 50 Ohm filter designs. The second is for higher impedance SAW designs that can be successfully matched to higher impedance first mixer collector loads, with minimal warping and insertion loss.

Since the first mixer requires high impedance loading to develop maximum conversion gain, 50 Ohms SAWs can be matched passively through reactive matching networks or actively through an external impedance transforming stage, such as an emitter follower. The latter case provides additional external IF gain to overcome high insertion SAW losses while providing a low impedance sourcing drive to the filter. An emitter follower also buffers the mixer output with a very high gain impedance to maximize conversion gain.

Some manufactures will make recommendations on suggested active networks optimal for driving their designs. Basically, one can provide the required inductive pullup for the first mixer output/s, tuned to the mixers internal 2 pF differential capacitance, or 4 pf single-ended capacitance. The Q of the resulting LC band pass can be set as determined by the unloaded inductor Q or a fixed resistive termination across the inductor/s. The current in the emitter follower can be set based on drive requirements and the supply voltage roughly as ie: = (Vcc-Vbe)/RE by selecting the emitter resistance RE. The effective emitter follower source impedance to the filter or and additional stepup network on the input of the filter will be determined roughly as the equivalent LC Q loading resistance divided by beta, in series with the effective intrinsic emitter resistance re = Vt/Ie. An additional resistive buildout can be used to adjust/stabilize this sourcing impedance to the SAW filter. The impedance of the emitter follower can be set in this manner to values less than 50 Ohms if followed by a reactive stepup network, such as an inductor, into the SAW input. The emitter follower can dump additional power into such a low impedance load to overcome high SAW filter insertion loss.

The following design procedure can be followed when implementing a passive reactive match to a SAW filter into the design.

Table 17 SAW Filter Characteristics

Centre Frequency	Input Impedance	Output Impedance
41.82 MHz	550R // 19 pF	370R // 21 pF

In this example we are assuming our main objective is to power match the filter and to improve conversion gain by adding a series capacitor. It would be possible to match the filter with just a single inductor but this would result in low conversion gain and is more likely to impact on system Noise Figure. The following design steps are taken.

1) Model the high input impedance matching circuit (including the first mixer bias pull ups and internal capacitors) which transforms to the desired SAW input impedance goal.

2) Simultaneously and iteratively model the associated SAW filter output impedance and transform to an appropriate second mixer input impedance. Generally, optimum second mixer noise figure performance will be found driving from a 1.5 k Ohms source. However, other consideration, such as component count and stability, could result in other choices, which are made feasible by the optimal noise figure provided by the second mixer.

3) Calculate the voltage conversion gain of the first mixer from the real part of the modeled mixer loading impedance, Rlmix. Convert this to power conversion gain by subtracting 10log (Rlmix/50 Ohm).

4) Confirm through calculation that you have realized sufficient power gain, prior to the SAW filter, to ensure that the cumulative system noise figure is not significantly degraded due to the high insertion loss of the SAW filter.

5) Confirm through measurement that acceptable -3 dB sensitivity and system noise figure have been realized.

In exactly the same way as the matching circuits were designed for the RF path in Section 3.2 on Page 22, the L and C matching can be derived using the EEZMatch software. Using the SAW filter described in Table 17 a matching network was derived within EEZMatch the results of which are shown in Figures 19 and 20.

- Mixer1 Output Match

- CKT
- CAP 22 0 C=19.0 ! C37 C=PF
- CAP 22 23 C=27.0 ! C38 C=PF
- IND 23 0 L=820.0 ! L13 L=NH
- CAP 23 0 C=5.5 ! C39 C=PF
- RES 23 0 R=4309.0 ! R10 R=OH
- R = Equiv parallel loss resistance of L
- R = 2 x PI x Freq x L x Q = 4309R (Q ~ 20)

- From Chart
  - *Load = 18.25 * 50 = 913R*
  - *Y21(mixer1) = 0.0593 A/V*
  - *Conversion G = Y21/2 x Load*
  - *Conversion G = 27.07 vdB*
  - *Impedance Change 50R to 550R*
  - *10 log (550/50) = -10.4dB*
  - ***Total G = 27.07 - 10.4 = 16.67 vdB***

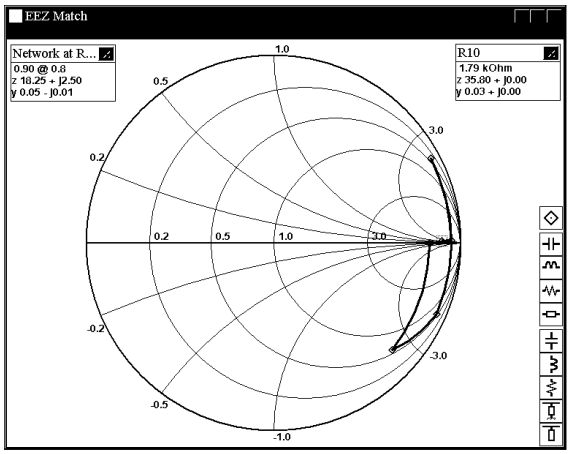


Figure 19 SAW Filter input Match to Mixer1 Output

- Mixer2 Input Match

- CKT
- CAP 22 0 C=21.0 ! C40 C=PF
- CAP 22 24 C=12 ! C41 C=PF
- IND 24 0 L=1000.00 ! L14 L=NH
- CAP 24 0 C=5.62 ! C42 C=PF
- RES 24 0 R=5225.0 ! R12 R=OH
- R = Equiv parallel loss resistance of L
- R = 2 x PI x Freq x L x Q = 5225R (Q ~ 20)

- From Chart
  - *Load = 39.2 * 50 = 1960R*
  - *Mixer2 Input Z = 2K*
  - *Hence matches Mixer2 Input*

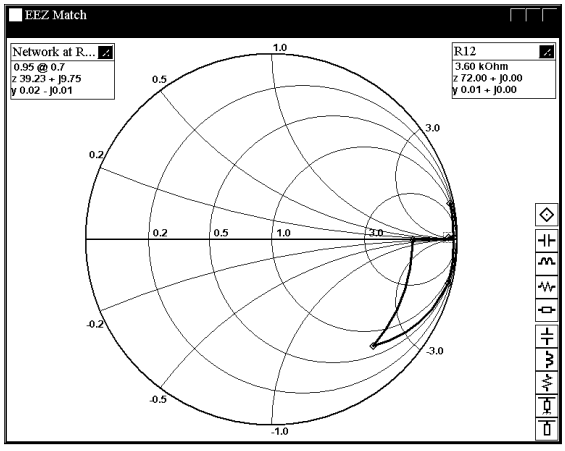


Figure 20 SAW Filter Output Match to Mixer2 input

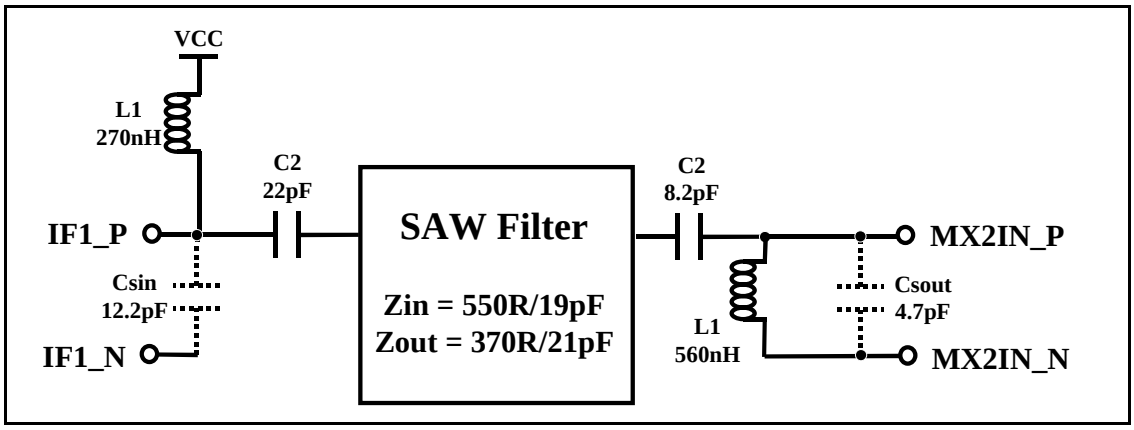


Figure 21 Circuit Implementation for 41.82 MHz SAW Filter

The following calculations were used in simulating the matching network in EEZMatch. The calculations for the SAW filter input match are demonstrated here, Given L = 820nH with self resonant frequency,

$$Cleq = 1/(L \times (2 \times \pi \times Fres)^2) = 1pF$$

(Fres) @ 180 MHz and typical Q of 20 at 40 MHz. To determine the inductor equivalent parallel resistance,

$$Rleq = 2 \times \pi \times L \times 41.82MHz \times Q = 4309R$$

Given that the Mixer1 output has an internal load capacitance of 4 pF and allowing 0.5 pF for stray effects we can estimate the total load capacitance at the output of Mixer1,

$$Cshunt = 4pF + 0.5pF + 1pF = 5.5pF$$

The Smith chart shown in Figure 19 on Page 53, provides a network impedance which is presented to the Mixer1 output. Calculations are provided in this diagram using the specified transconductance of Mixer1 to determine the voltage conversion gain. The conversion gain achieved is approximately 27 dB V, which is reduced to approximately 16 dB V once the impedance transformation is accounted for. Exactly the same process is applied to matching the SAW filter output only in this case the primary concern is in matching the 2 kOhm load characteristics of the Mixer2 input. From the example shown, in Figure 20 on Page 53, a very good match is realised.

3.7 Reference Clock

The reference clock, typically a TCXO, is required by both the UAA1570HL and SAA1575HL. It is divided down by the UAA1570HL and used by the PLL in generating the first local oscillator at nominally 1.5336 GHz. It is also divided down by the SAA1575HL and used as a clock to sample the IF data from the UAA1570HL.

For the EXACT GPS system the following oscillator specification is recommended,

Table 18 Recommended Specification for Reference Oscillator

Label	Value	Comments
Frequency	14.40 MHz	Software written for this reference frequency
Preset Frequency	±0.5 ppm	Typical TCXO specification
Temperature Stability	± 5 ppm	Most TCXO's well within this range. The most important factor is a **Total Tolerance of ± 15 ppm over lifetime.**
Ageing	± 1 ppm/year	See Comments Above
Output Waveform	1 V p - p (minimum)	In order to maximise VCO phase noise performance it is important to provide at least a 1 V swing at the reference I/P
Output Load	10 k//10 pF	Typical Load Rating
Phase Noise	-130 dBc/Hz @ 100 Hz -140 dBc/Hz @ >500 Hz	If significantly worse than this, ie: VCXO, it will impact on the VCO phase noise of the system.

3.7.1 UAA1570 Considerations

The most critical aspects of the reference oscillator are the impact on the VCO phase noise and the frequency stability over lifetime. Another very important issue is thermal and physical shock compensation. If the oscillator frequency is allowed to drift quickly either through rapid temperature variation or physical shock the likelihood is that satellite tracking will be lost momentarily. RAKON have a number of proprietary production techniques which greatly reduce the susceptibility of the oscillator to shock and vibration. They have also developed test facilities which improve their ability to eliminate devices which exhibit frequency perturbations not generally identified by other crystal manufacturers. At the time of producing the reference design Golledge oscillators were used primarily for reasons of cost although RAKON devices were also verified in the final system.

In order to maximise the VCO phase noise performance it is recommended that the oscillator phase noise is better than -130 dBc/Hz at an offset from carrier of 100 Hz. This is usually within a typical TCXO specification but not always achieved by VCXO's. The UAA1570HL has an internal squaring circuit so the reference source should be AC coupled to the IC. This has been chosen at 4.7 NF, which is low impedance at 14.4 MHz.

The amplitude of the reference is ideally between 1 V p - p and 1.5 V p - p. The internal DC reference is nominally at Vcc - 1 V, therefore some care needs to be taken to avoid clipping the supplies. The Golledge parts are specified at a minimum of 0.8 V p - p, providing nominally 1.4 V p - p.

The SCLK input is internally biased to half the supply, and has internal gain and squaring circuits. The amplitude of the signal can be as low as 20 mV p - p but must not have a peak value greater than 0.75 Vcc. In order to achieve this a divider network is required from the output of the SAA1575 to the input of the UAA1570 as shown in Figure 22 on Page 56.

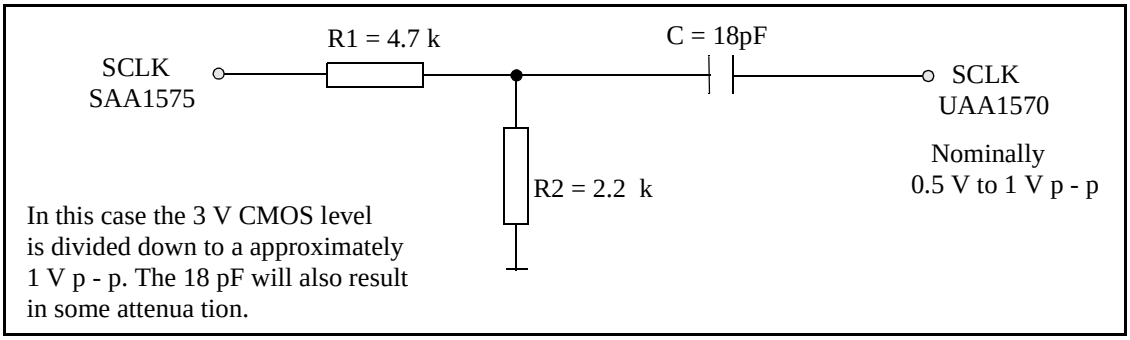


Figure 22 SCLK Divider Circuit for UAA1570

Table 19 Reference Clock and Sample Clock Limits for UAA1570

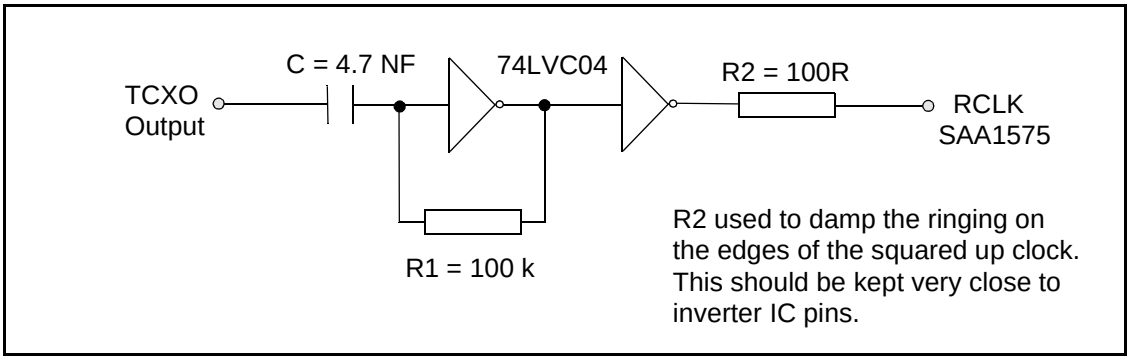
	Vcc = 5 V	Vcc = 5 V	Vcc = 3 V	Vcc = 3 V
Clock	**Minimum**	**Maximum**	**Minimum**	**Maximum**
RCLK	100 mV p - p	1.6 V p - p	100 mV p - p	1.7 V p - p
SCLK	20 mV p - p	2.4 V p - p	20 mV p - p	1.5 V p - p

Note: clock voltages refer to the UAA1570 specifically in Table 19. Where the UAA1570 and The maximum SCLK input voltage swing should not exceed 75% of the supply. All supply and SAA1575 supplies are different the levels should be referenced to the lesser of the two supplies.

3.7.2 SAA1575 Considerations

The reference clock must be squared up prior to input to the SAA1575. This is divided down internally to provide a 4.8 MHz clock for sampling the IF data from the UAA1570. The SCLK output is divided down for input to the UAA1570 as described in the previous section. The RCLK input on the SAA1575 has no internal squaring circuit so this must be down externally and on the reference application a standard 74 series inverter is used to do this.

An important consideration at this stage is that the 3rd harmonic of the 14.40 MHz reference clock falls essentially in the first IF passband. It is essential that this harmonic has minimal effect on the overall system noise figure. Much of this can be achieved by providing common mode rejection in the first IF filter as described in Section 3.4 on Page 37, but also by careful layout as described in Section 4.5 on Page 70 and Section 4.6.



3.8 Digital Interface

This section covers the circuit considerations related to the interface between the UAA1570 and the SAA1575. The three interfaces are the serial communications, sample clock and IF data.

3.8.1 RF Serial Interface

The serial communications interface has two main functions. The first is to allow the frequency plan of the UAA1570 to be programmed. The Philips reference design uses the default settings for the UAA1570 eliminating the need to wire this interface on the board. The second purpose is to allow the UAA1570 to be placed into partial or full power down mode.

Care must be taken when using this interface when the two devices are being run at different supplies. Typical applications would normally be implemented on a single supply configuration, however there may be some cases where the SAA1575 is run on a 5 V supply with the UAA1570 running from 3 V. In this instance a voltage divider would be required on each line of the bus to divide the 5 V CMOS levels down to 3 V for the RF IC.

In order to guarantee that the UAA1570 default frequency plan is programmed it is important that the RFLE line, pin23, is held low on the UAA1570. This should guarantee that no data is spuriously programmed into the RF device. It is recommended that all three interface lines are tied to ground when the default frequency plan is used.

The serial interface can be used to invoke a full or partial power down of the UAA1570. It is possible to set registers which can power down either the whole IC or alternatively only power up the VCO and PLL circuitry. This feature is not implemented in the current EXACT firmware.

3.8.2 SCLK and SIGN Output

The SCLK considerations have been discussed in some detail in 3.7.1. The main consideration is to AC couple the SCLK to the UAA1570 limiting its peak voltage swing to 2.4 V in a 5 V application and 1.5 V for a 3 V application. Where the UAA1570 and SAA1575 supplies are different the levels should be referenced to the lesser of the two supplies.

The intention was for both the UAA1570 and SAA1575 to be run at the same supply voltage. This would make all the interface issues much more straight forward. In this instance if power consumption was a serious concern then the designer is more likely to run the system from an all 3 V supply. The biggest problem with the IF data interface, (SIGN), from the UAA1570 to the SAA1575 is if the RF IC is running at a lower voltage than the baseband. In the example below we assume UAA1570 is at 3 V and the SAA1575 is run at 5 V. In this case a level shifting network would have to be implemented to guarantee the functionality in a production environment.

- SAA1575 minimum input Hi level = 0.7 Vcc (3.5 V)
- UAA1570 minimum output Hi voltage = 1.794 V

If we AC coupled the SIGN output and then used a resistor divider network to shift the SIGN output to a 2.5 V DC reference the minimum possible SIGN output amplitude would only be 3.397 V.

- ie: 2.5 + (1.794/2) = 3.397 V

Therefore although this configuration would work a very high percentage of the time it would not be complying with the worst case specification data and could therefore not be guaranteed in production. If the two devices are to be run a different supply voltages then a level shifting circuit should be used.

3.9 Clock Circuits for SAA1575

The SAA1575 has two main clock circuits, the system clock at 30 MHz and the real time clock at 32.768 kHz. The real time clock circuit is a standard application and does not require any detailed explanation.

3.9.1 30 MHz System Clock

The three most important issues related to the system clock design are as follows:

- Meeting transconductance characteristics of oscillator for start-up performance
- Meeting crystal load capacitance rating in the chosen application
- Meeting power dissipation rating of crystal.

Table 20 SAA1575 System Clock Oscillator Characteristics

Transconductance gm	XTAL1 I/P (Lo)	XTAL1 I/P (Hi)
9mS	0.22 PVcc	0.7 PVcc

The SAA1575 oscillator characteristics are shown in Table 20. The transconductance rating is a nominal measurement and not a minimum limit. The first step is to choose a crystal whose load capacitance rating results in a design that at worst case start-up conditions falls within the transconductance rating of the SAA1575. In this case a standard 20 pF load capacitance rating gave a reasonable result. Standard formulae are provided which enable the gm requirements of the circuit to be estimated at worst case start-up conditions as well as typical and worst case nominal running conditions.

- Formulae
- gm(typ) = esR(typ) * C1*C2 * {(2*pi*Freq)^2} * { (1+Cp(C1+C2)/C1*C2)^2}
- gm(min)start-up = 3 * esR(max) * C1*C2 * {(2*pi*Freq)^2} * { (1+Cp(C1+C2)/C1*C2)^2}
- gm(standard) = 4*esR(max) * Cload^2 * (2*pi*Freq)^2
- Model of Crystal Circuit
- Key:
- gm = transconductance
- Co = Shunt Cap (Xtal)
- Cx1 = Ext I/P Cap
- Cx2 = Ext O/P Cap
- esR = Xtal Series R
- Cfb, Cstray1, Cstray2 are stray capacitor effects

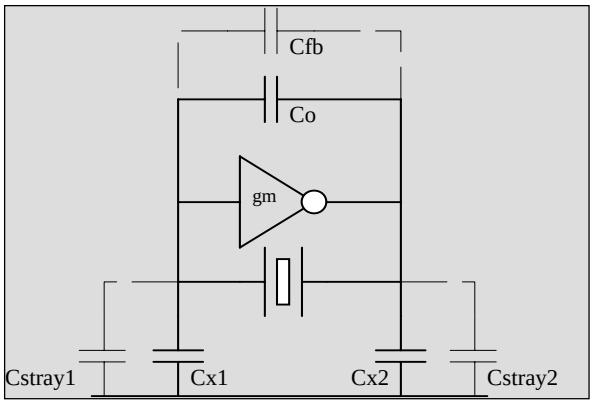


Figure 23 Determining 30 MHz Oscillator Circuit Requirements

In the formulae for gm the following apply:

- Cp = parallel combination of Co and Cfb
- C1 = parallel combination of Cx1 and Cstray1
- C2 = parallel combination of Cx2 and Cstray2.

In the reference design a Golledge crystal was used with the specification outlined in Table 21 on Page 60.

Table 21 Specification for 30 MHz Crystal

Parameter	Rating
Golledge Part Number	GSX-1B 30.00 MHz
Frequency	30.00 MHz ± 100 ppm
Maximum Drive Level	0.1 mW (Maximum)
Load Capacitance	20 pF
Shunt Capacitance	7 pF
Series Resistance (ESR)	40R (Maximum)
Estimated Nominal ESR	20R (Not specified by Golledge)

In this case the stray capacitance effects have been assumed to be in the order of 2 pF and the load capacitors chosen at 22 pF. When all the data is input into the equations it yields a circuit load capacitance close to the 20 pF rating of the crystal and a worst case gm requirement at start-up at least 10% below the nominal gm of the SAA1575.

Results from equations:

- Cp = 9 pF C1 = C2 = 24 pF Cload = 21 pF
- gm(typ)run = 1.25 mS gm(min)startup = 7.52 mS

The power dissipation in the crystal can be determined by measuring the voltage across the crystal in the final application and calculating the consequent drop across the series resistance of the crystal. In the reference design the voltage drop across the crystal is approximately 0.5 Vrms. The reactive impedance of the shunt capacitor, 7 pF, at 30 MHz is 758R which at resonance is the impedance of the LC network in series with the ESR of the crystal. Therefore the voltage across the crystal series resistor is 25 mV.

$$Vr = (0.5 \times 40)/(758 + 40) = 25.1\text{mVrms}$$

This yields a typical power consumption of the crystal of 16 μW which is well within the limits of the crystal.

$$Pxtal = (25\text{mV})^2/40 = 15.7\text{uW}$$

In the final application a bias resistor of 100 k is used across the oscillator. This is recommended but not mandatory and is used to guarantee the oscillator is DC biased correctly. The series resistor at the output of XTAL2 is optional in this application. It can be used to control power dissipated in the crystal and also provides some high frequency filtering in conjunction with CXtal2.

3.9.2 Real Time Clock Oscillator

The real time clock application is standard. A typical watch crystal with nominal 27 pF load capacitors is implemented in the reference design. The specification for the crystal used is shown in Table 22 on Page 61.

Table 22 Watch Crystal Specification

Parameter	Rating
Seiko-Epson Part Number	MC-406 32.768 kHz
Frequency	32.768 kHz ± 50 ppm
Maximum Drive Level	1.0 µW (Maximum)
Shunt Capacitance	12.5 pF
Series Resistance (ESR)	50 k (Maximum)
Estimated Nominal ESR	20R (Not specified by Golledge)

3.10 Power Up/Down Control for SAA1575

The power up and reset behaviour of the SAA1575 is very important and great care needs to be taken to ensure this is done correctly. The reset lines are used to detect imminent power failure and initiate a safe memory backed up power down sequence, as well as ensuring safe rest and stabilisation at power up. One of the main issues is ensuring successful reset when the SAA1575 supplies are split between 5 V and 3 V.

3.10.1 Power Up Sequence

The power up and reset relates to the following pins of the SAA1575,

- PWR_FAIL and PWR_DN — Usually driven by voltage detectors
- RSTIME — Dictates stabilisation time for oscillator
- PWRB and PWRM — Control lines for battery backup switch

Table 23 Power up Procedure for SAA1575

State	Description
Power Off	In this state main power is not applied. If used, a battery backup circuit will maintain power to BVcc and RVcc for the memory and real time clock. This circuit will be controlled by PWRM and PWRB. In this instance PWRM will be Hi with PWRB Lo.
Main Power Applied	The main system power is ramped up. At this stage PWR_FAIL and PWR_DN are both held low, usually via voltage monitor circuits. Nothing should change until the main power is up to threshold, ie: 0.7 of CVcc.
IC Reset	Once the core supply CVcc is above its nominal threshold PWR_FAIL must remain low for up to 100 μS. For safety it is recommended that this delay is kept to at least 1mS. At this stage the IC is held in a reset state until PWR_FAIL goes Hi.
Backup Power Handover	In the reference system design PWR_FAIL is set to go high at around 2.6 V. When PWR_FAIL goes high it immediately switches PWRM and PWRB which in turn will switch the memory and real time clock supply over to the main system power.
RSTIME PWR_DN goes Hi	At this stage the battery power is disabled and the system is running from the main power supply. PWR_DN is set to go Hi at 2.9 V on the reference system design. When this goes high a timer is set and its duration dictated by the RSTIME input. Reset is deserted after this delay and the first program memory strobe is sent to access the EPROM. RSTIME Lo delay = 1 mS (Intended for external clock input to SAA1575) RSTIME Hi delay = 10 mS (Typical application when using an on board XTAL)

Table 23, outlines the power up procedure for the SAA1575. The most critical aspect of the design is when the core supply, CVcc is run at nominally 3 V with the peripheral supply, PVcc run at 5 V. In this instance we need to guarantee that the core supply is up to the nominal threshold at least 1 mS before PWR_FAIL goes high. In cases where the core supply is run at a lower voltage to the periphery supply it is sometimes better to use a fixed hardware delay on the PWR_FAIL line of nominally 10 mS. This ensures that if the core supply has a long rise time that PWR_FAIL does not go high prior to the core supply getting up to its nominal threshold level.

3.10.2 Power Down Sequence

The power down sequence is essentially a complete reverse procedure of the power up sequence. The critical issue here is in allowing some delay between PWR_DN and then PWR_FAIL going low to allow the software to execute a safe memory backup procedure before the IC goes into reset.

Table 24 Power Down Procedure for the SAA1575

State	Description
Power Drops PWR_DN goes Lo	If the supply drops below the threshold of PWR_DN, in this case 2.9 V, then PWR_DN will go Lo activating an interrupt to the SAA1575. This interrupt causes the software to stop executing from program memory and backup data to memory. Once this is down it forces the IC into a software reset.
Imminent Power Fail PWR_FAIL goes Lo	Once the supply drops below 2.6 V PWR_FAIL will go Lo, on the reference design this is controlled by a MAXIM voltage detector. When PWR_FAIL goes Lo it immediately switches state of PWRM and PWRB allowing power to be maintained by the backup battery. PWR_FAIL going Lo also forces the IC into reset.

The maximum time required by the software backup routine is not clearly specified. This depends mainly on the time required to complete its current task before backing up memory and safely putting the IC into reset. It is anticipated that this is never likely to be more than a few hundred micro seconds so again we suggest a delay of at least 1mS between PWR_DN and PWR_FAIL going Lo is designed for.

3.10.3 Split 5 V and 3 V Supply Considerations

The issue of mixed supplies is covered briefly in Section 3.8 on Page 57. One of the main concerns is guaranteeing that PWR_FAIL remains Lo for at least 1 mS after the core supply is up to its nominal threshold level. If the core supply has a long rise time relative to the PVcc supply which is often the case, it is advisable to fix a hardware delay to the PWR_FAIL line as indicated in Figure 24.

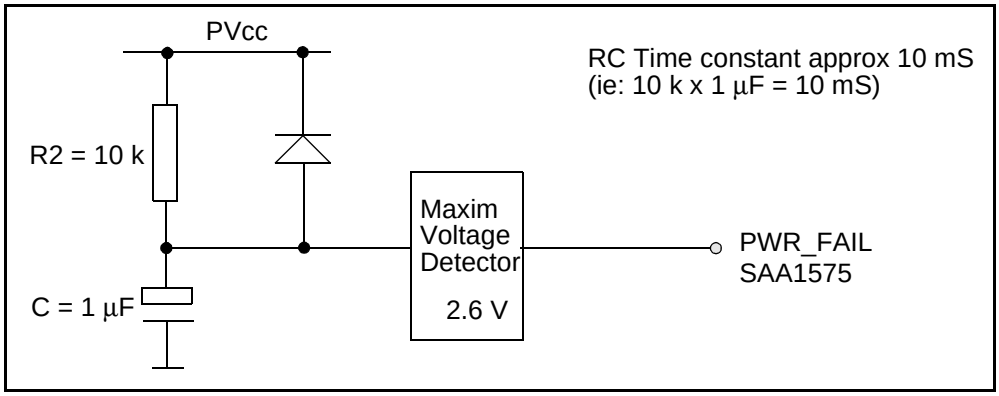


Figure 24 PWR_FAIL Delay Circuit for Mixed Supply Applications

3.11 Battery Backup Circuit

The battery backup circuit uses simple transistor circuits to switch power from the main supply to battery supply under power failure conditions. The backup circuit can be controlled by the lines PWRM and PWRB which are set by PWR_FAIL directly.

- PWRM Switches to main supply and is active Lo
- PWRB Switches to battery supply and is active Lo.

An alternative to a discrete transistor solution is to implement a microprocessor supervisory circuit but these are generally going to be expensive especially compared to the design used on the reference system. The main issue related to the design is again that of using mixed 5 V and 3 V supplies for the SAA1575. In this report the two common applications are discussed which are the all 3 V design and mixed 3 V and 5 V design.

3.11.1 Single 3 V Application

The battery backup circuit for the single 3 V solution is very simple and consists of 2 transistors and some bias resistors, driven directly from PWRM and PWRB, as shown in Figure 25. In this design the 1 M bias resistor for the battery backup switch is chosen primarily to minimise the power consumed in the bias itself. This application is employed on the reference design and yields a typical backup supply current of nominally 13 μA at 3 V or approximately 40 μW.

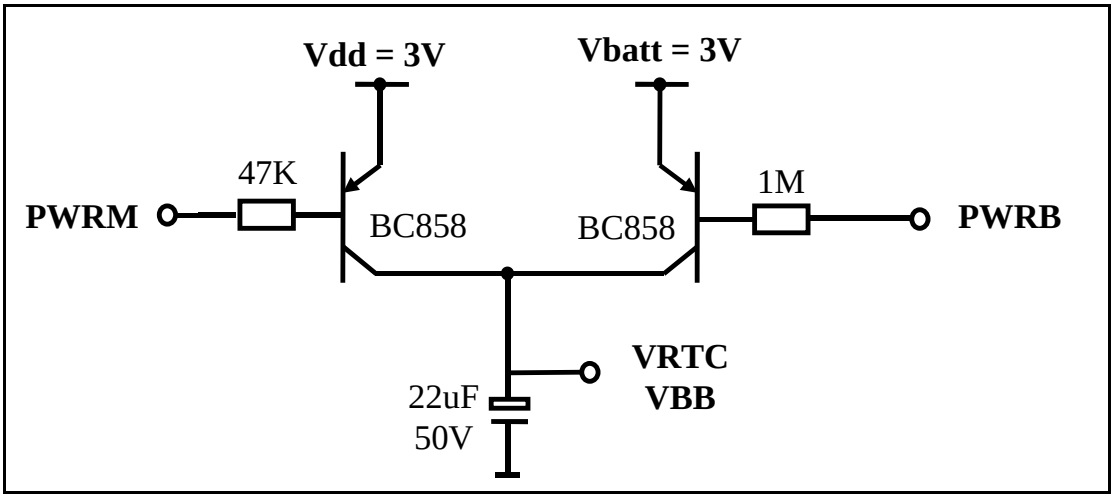


Figure 25 Battery Backup Circuit for Single 3 V Supply

3.11.2 Split 3 V and 5 V Application

The battery backup solution required for the mixed supply application is a bit more complicated. In this instance we have to isolate the drive to the main power switch from PWRM. This is because in backup mode PWRM is powered from the battery supply at nominally 3 V. Consequently the conventional all 3 V circuit would mean that in backup both output switches would be on leading to partial powering up of the GPS system. The secondary issue is that the memory will be powered nominally from a 5 V supply under normal conditions so the RVcc and BVcc supplies need to be provided separately. Figure 26 on Page 65 shows a practical discrete solution for this application.

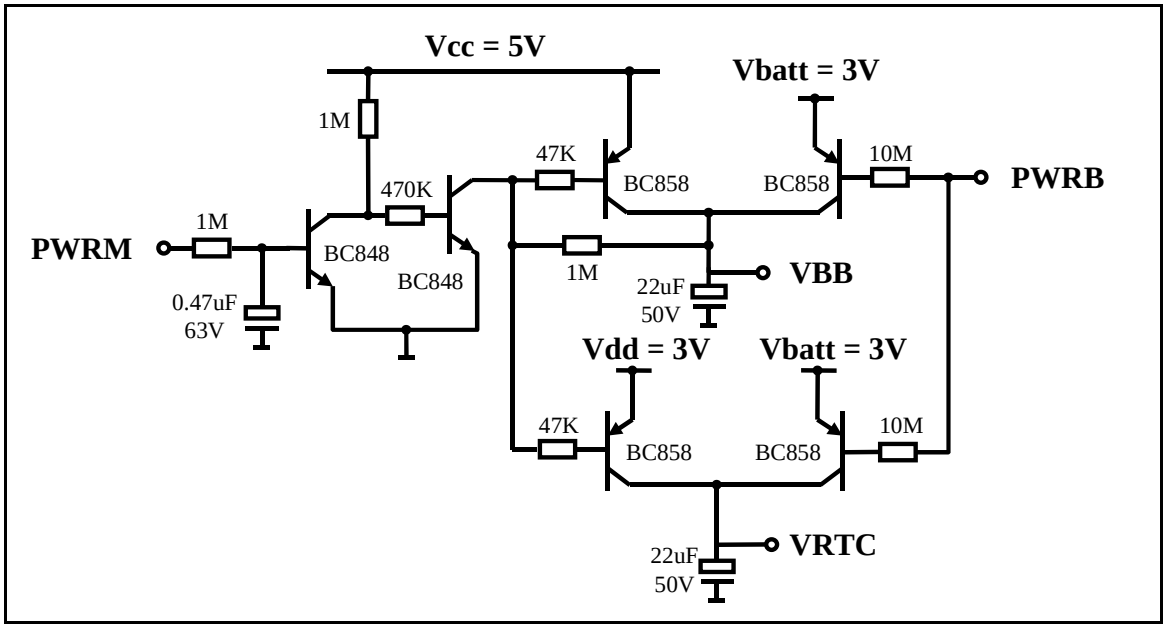


Figure 26 Battery Backup Circuit for Mixed 3 V and 5 V Supplies

4 GPS ENGINE LAYOUT GUIDELINES

This section considers each system element in turn and highlights the critical layout aspects of each. In many cases there is often a trade off between ideal layout requirements and board size constraints. For this reason Section 4.1 attempts to identify the most critical areas of the layout that should be given the highest priority and considered before the layout of the board commences.

4.1 Summary of Critical Layout Areas

Each of the areas listed here are covered in detail separately within Section 4. Table 25 provides an overview of the most critical layout aspects of the design together with symptoms resulting from poor layout. It is strongly advised that attention is paid to these issues prior to commencing layout as well as referring to the associated guidelines later in this section.

.

Table 25 Overview of Most Critical Layout Aspects Of Gps Design

Circuit	Layout Guidelines	Symptoms of Poor Layout
RF Microstrip Layout	Ideally microstrip lines kept straight Avoid close proximity components Avoid close proximity GND strays Serial vias should be avoided in matching network except in shunt at LNA o/p pins LNA o/p's need extremely close proximity fractional capacitance	All lead to gain loss through poor matching If impossible to avoid in layout the stray effects introduced must be carefully modelled and thus accounted for in the design
VCO and Loop Filter	Use high Q resonator inductor (0805 minimum) Close proximity layout at corner of IC Low impedance GND return to Pin11 Short routing to minimise inductance Loop filter close to Pin40 with low impedance GND return to Pins 38 or 42	Wideband phase noise and resulting correlation jitter high and LO1 squared noise will degrade MX1 Noise Figure Many of these can indirectly lead to failure of VCO Common problem is track inductance being too high. Can be overcome by reducing L in the circuit but aim is to keep this as high as possible
Reference Clock	Avoid vias especially exposed ones Trace lengths as short as possible Coplanar shield clock lines and/or route on inner layer of board Keep well clear of all IF stages	Can ultimately limit the -3 dB sensitivity and system Noise Figure Main issue is to minimise high frequency harmonics getting into the IF stages
General Digital and Analogue GND isolation	Isolate GND planes back to supply input Duplicate isolation on all layers	Can introduce digital noise into RF degrading the VCO phase noise response
Analogue and Digital 14.4 MHz GND Isolation	Run all digital and analogue grounds into dead end branches, from input connector No shared GND loops Make a small link between digital and analogue GND's on one layer only, directly between the TCXO and Inverter stages	Shared digital current return paths, especially 14.4 MHz reference GND plane will degrade VCO phase noise This minimises radiated emission of the 14.4 MHz clock harmonics and minimising level of 3rd harmonic in first IF stage

Table 25 Overview of Most Critical Layout Aspects Of Gps Design (Continued)

Circuit	Layout Guidelines	Symptoms of Poor Layout
Digital and Analogue Supply Isolation	Run all digital and analogue supplies into dead end branches from input connector Provide a minimum 15 μF tantalum bypass position on each isolated supply branch	Shared digital supply lines with RF or in particular with the reference clock will be fatal Analogue/Digital supply proximity can induce undesired coupling

4.2 Microstrip Line Layout

The layout of the RF matching networks is to some extent the most critical part of the layout. If this is not done carefully the impedance matching goals will not be achieved, resulting in low RF gain and poor system NF, and at worst case preventing the system from acquiring satellites at all. Some of the key issues involved are listed here:

4.2.1 Avoid Close Proximity Stray Grounds Pertubations

- Close proximity (short RF grounds via paths) are very desirable, but avoid stray undesired/unintended perturbations of close by microstrip lines. Always add excess RF grounding vias in all RF plates and near all RF components. Always use excessive RF ground plane, avoiding pinched plates.
- Capacitive and inductive coupling as a result could lead to poor impedance matching.
- If possible try to maintain a clearance between the microstrip and associated ground fill of at least 4 times the given track width.
- Leave reasonable ground clearance around the RF connector centre pin on all PCB layers. This helps to eliminate capacitive coupling effects. If too wide a gap is left the coupling can become inductive but this is more easily corrected by adding a small capacitance directly at the connector pin.

4.2.2 Avoid Close Proximity Components

- All matching lines and components should be kept well away from the VCO. The signal traces and decoupling components for the VCO carry high signal currents around the loops which we need to avoid introducing into the RF amplifier stages.
- Close proximity components can result in capacitive or inductive coupling which can upset the impedance matching objectives and realized RF gains or lead to coupling of stray signals into unassociated system block functions. Always isolate components by function - never intertwine RF/IF/DIG functions.

4.2.3 General Microstrip Layout Guidelines

- All microstrip lines should be kept as straight as possible. Any bends in the line can alter the characteristic impedance and result in mismatch.
- Serial vias should be avoided in the RF matching layout. If this cannot be avoided then the properties of the via need to be carefully modelled in the network design prior to layout.
- Both LNA outputs require close proximity fractional capacitance to achieve the matching goals of the design. In this instance a via directly at the UAA1570 pins can be used to connect to this shunt capacitance. In practice the required capacitance is so small that tolerances can have a significant effect. To this end on the reference design an open stub capacitance has been implemented to eliminate the need for a physical component. Refer to Section 3.2.4 on Page 29 for LNA2 Matching.
- All matching capacitors should have a good low impedance ground return.
- Microstrip lines MUST NOT be run under other components in the design.
- Ideally for a microstrip line to work properly it should pass over uninterrupted inner layer ground plane. However the UAA1570 is relatively easy to use since ample RF gain arrangements allow significant RF mismatch. That is as long as the first LNA has optimal input noise match with adequate gain, whether this LNA is internal and/or external - good system performance is almost guaranteed!

Great care must be taken to ensure the matching networks meet their goals. Failure to adhere to the guidelines described in this section will ultimately lead to a mismatched design which in turn is likely to prevent the system from operating at all. The early gain stages are critical to achieving acceptable receiver sensitivity performance and if badly designed is very difficult to recover in the latter stages of the signal path.

4.3 VCO and PLL Filter

The two fundamental issues regarding the VCO are the tuning range and overall phase noise response. As well as this it must be remembered that the VCO is running only 40 MHz below the RF input frequency. The signal currents being carried around the VCO application are very high and if picked up by the LNA stages may cause problems. Therefore it is important to keep the VCO circuit and RF gain stages as far apart as is reasonably possible.

The nominal operating point capacitance of the varactor should be minimized relative to the VCO negative impedance port effective internal series capacitance as specified in the data sheet. This maximizes the pulling effect the varactor capacitance will have on tuning range. This maximizes Ko (MHz/volt) and can be best optimised by using double varactor diodes in series. High Ko will allow wider resonator component production tolerances to be absorbed ensuring adequate lock voltage range margins.

The implemented series resonator structure provides a relatively linear Ko, while a parallel tuned resonator structure provides a nonlinear Ko and can be used to extend tuning range. Eventually, however, excessive Ko values can result in degraded stray tuning pick-up and result in phase noise degradation sensitivity.

4.3.1 VCO

The main objective in the VCO design is to achieve a nominal tuning voltage close to the middle of the overall tuning range. The value of inductor required can be determined by estimating the Ct of the resonator circuit at this voltage and calculating for a running frequency of 1.5336 GHz, as described in Section 3.3 on Page 34. In the reference design we have used a 5.6 nH inductor.

It is the overall inductance in the signal path that leads to the most problems in the VCO layout. The traces from the TANK pin of the UAA1570, through to the varactor are extremely critical. These traces add inductance to the physical inductor already placed and in turn pushes the required tuning voltage closer to its upper limit and at worst case complete VCO failure results. To safeguard against such problems the following layout guidelines should be followed:

- The resonator loop circuit, including the series inductor, series capacitor, varactor, and first resistor of the RCR tune network, should be kept as short and close as possible to VCO pins 9, pin 10, and pin 11. Do not use vias in this main resonator loop path. The associated inductance and capacitance can significantly transform the desired impedances.
- The traces used in the inductance path should be relatively low impedance. It is therefore recommended that the trace width is slightly increased in this path to minimise additional inductive properties.
- Avoid inadvertently injecting high level VCO signal into close proximity LNA microstrip lines or biasing decoupling components. The VCO decoupling capacitor should also be considered a high level source of VCO radiation.
- The VCO components should be kept as close together as possible to minimise stray effects. This forces the tuning to be dictated by the values of varactor and inductor only.
- The VCO resonator loop grounding return path, that is the varactor ground path to the VCO ground pin 11, should be as short as possible and structured using large/ wide grounding plates. This grounding plate should be directly attached to the VCO ground pin pad taking advantage of the fact that pins 12 and 13 are also RF grounds. That is keep the return path wide to minimize ground inductance.
- DO NOT USE VIAS. This must be avoided at all costs as it essentially increases the overall inductance in the signal path reducing the required value of the physical tuning inductor. At worst the VCO will not run and if it does the physical inductor will be so small tolerance effects may have a detrimental effect in production.
- The phase noise performance beyond the PLL loop bandwidth is dominated by the Q of the VCO resonator. Realizing a higher Q resonator allows the loop bandwidth to be closed at a narrower value. It is important that the integrated phase jitter over the PLL loop bandwidth not exceed 100mrads rms to prevent correlation losses in the receiver. Therefore, the minimum recommended size for the resonator inductor is 0805. Low resonator Q can also result in degraded first mixer noise figure performance through wideband LO white noise squaring (limiting) if the ultimate VCO noise floor degrades. By optimising resonator Q the peak VCO signal will provide at least a -138 dBc/Hz margin to the wideband noise floor into the first mixer upper switching maintaining the first mixer noise figure performance specification.

4.3.2 Phase Locked Loop Filter

The loop filter components provide bandwidth control and consequently out of band attenuation to optimize VCO phase noise response. These components should be placed as close as possible to the COMP output at Pin40, with a low impedance ground return directly to pins 38 or 42.

However, avoiding coupling of digital noise into the loop filter components through direct radiation and preventing the charge pump pulse harmonics from radiating out into nearby IF components may necessitate a compromise. Distributing the loop filter components further along the tune line towards, or mingled with, the series resistor and shunt capacitor of the RCR tune low pass network, is an acceptable trade-off. Particularly if it minimizes potential undesired coupling. Every effort is made to minimize the total length of the resulting tune line structrure(s)) as this will also minimize the coupling potential.

4.4 First and Second IF Filters

In the reference design, as with many other programmable frequency plans, harmonics of the reference frequency can fall within or close to the first IF. This can be avoided by the choice of frequency plan, selecting those which offer the best immunity. The optimum choice with respect to this issue is to select a plan that results in the harmonics of the reference falling exactly at the second LO frequency. Since this is not always possible due to other constraints, such as a fixed reference frequency like the 14.4 MHz used in the reference design, the following recommendations should be followed as much as possible to insure the system does not become self jammed.

- Keep the filter layout symmetrical and compact. The best way to achieve this is by routing the first half of the filter outwards on one side of the PCB and then route the second half of the filter on the opposite side of the board moving in towards the Mixer2 input pins. The filter symmetry will mean any stray effects are common to both sides of the filter and keeping the layout compact makes it easier to isolate it from noise sources.
- Keep the filter well away from any high frequency radiation sources, especially the reference and sample clock in this case.
- If possible shield the IF filter with surrounding ground fill.
- Try to provide as much inner layer ground plane under the filter as is possible.
- Do not route signals or ground fill under any of the inductors. This can reduce the Q and lower self resonance of the inductor.
- If vias need to be used it is important to place these carefully in the layout. Closely spaced filter input and output vias can couple signals past the IF filters at high frequencies and or offset balance - defeating the purpose of the filter.

4.5 Reference Clock

The main purpose of the TCXO is to provide a reference clock source for the phase comparator of the UAA1570. This makes it very much an integral part of the RF application and should be kept relatively close to the REFIN pin of the IC and its associated ground return. However this clock is also used by the SAA1575 to provide a sample clock for retrieving IF data from the UAA1570, which in effect makes an integral part of the digital design also.

The goal here is to completely isolate the digital and RF layouts with the major concern being optimal phase noise response of the VCO. Perhaps the best way to achieve this is to position the TCXO and the digital squaring circuits reasonably close to the input power connector. By doing this they are both positioned close to the natural ground star point of the system, which provides two key benefits. Firstly they remain isolated from critical areas of the design and secondly a good low impedance ground return between the TCXO and squaring circuit minimises radiated emissions of the reference clock which can get into the IF stages.

The following recommendations for layout should also be followed as far as possible.

- TCXO must be well clear of the IF filter stages. Ideally position TCXO and digital squaring circuits either side of GND isolation to allow a single low impedance GND return to be provided between the two elements only, on one layer of the board.
- AVOID UNNECESSARY VIAS. Exposed vias are a source of radiation and must be avoided. Where vias do have to be used try to shield them by placing under the TCXO itself for example. It is essential that such vias are kept well away from the IF filter stages.
- Ideally route the reference clock on the inner layer furthest from the IF stages of the design. This allows ground shielding either side of the signal from the TCXO directly to Pin8 of the UAA1570. Ground vias should be interspersed along this shielding to all layers.
- The signal traces around the squaring circuit up to the RCLK input of the SAA1575 should be kept as short as possible. If long trace lengths are required it is advisable to route these on an inner layer furthest from the IF stages of the UAA1570 layout.

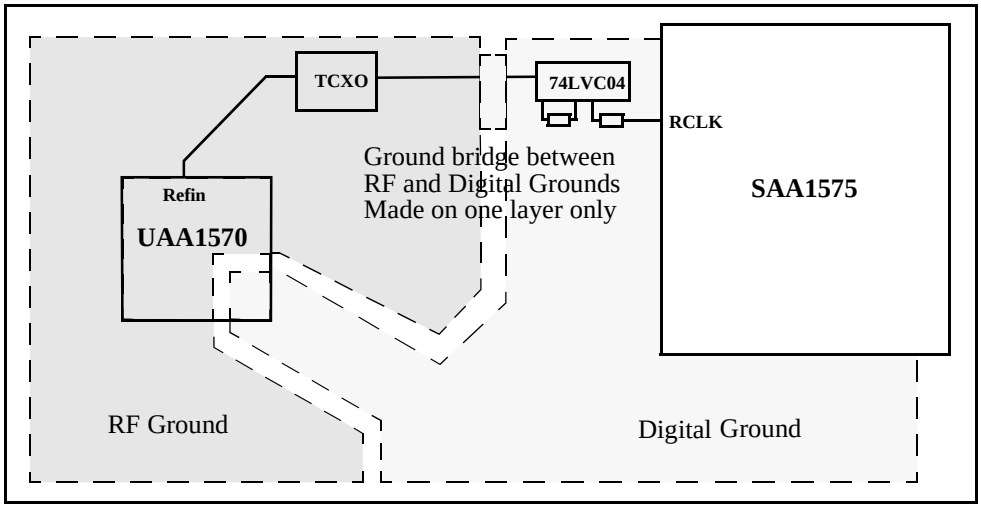


Figure 27 Layout Principle for Reference Clock Routing

Figure 27, helps to demonstrate this layout principle. The TCXO and Inverter are in themselves isolated from one another. However the small bridge between the two ground planes forces reference clock return currents along this low impedance path away from critical IF stages of the design. By minimising the ground return loop area it has the knock on effect of limiting emitted radiation that could otherwise get into the IF filters.

4.6 Digital Interface

In the reference design the serial interface for programming the UAA1570 is not required. Therefore the main concern is in the routing of the sample clock and IF data itself. The unused programme pins on the UAA1570 should be grounded in the reference design which uses the default frequency plan. Although it is advised that all serial lines are grounded on the UAA1570, it is only strictly necessary for the RFLE to be grounded to ensure the default frequency plan is implemented.

4.6.1 RF Serial Interface

This interface is not used on the reference design although provision has been made for this in case a need arises in the future. If implemented it is advisable to route these signals along the same path as the SCLK and SIGN signals between the UAA1570 and the SAA1575, as described in Section 4.6.2.

If the SAA1575 is running at a higher voltage than the UAA1570 the resistor divider networks for this interface should be kept close to the pins of the SAA1575.

4.6.2 Sample Clock and SIGN Output

These are the main interface lines between the SAA1575 and UAA1570. It is recommended that the digital and RF layouts are isolated on all layers of the board. The UAA1570 has a digital section which is isolated internally from the rest of the IC, which in the layout is taken as part of the overall digital layout. For maximum stability the digital supply and ground for the UAA1570 should be supplied from the digital baseband supplies and ground, using the isolated interface routing channel shown in Figure 28. Note also that the decoupling capacitor associated with these pins is therefore also returned and isolated in these planes.

It is proposed that the SIGN and SCLK signals are routed on an inner layer furthest from the RF layout with ground fill shielding from source to destination, as indicated in Figure 28.

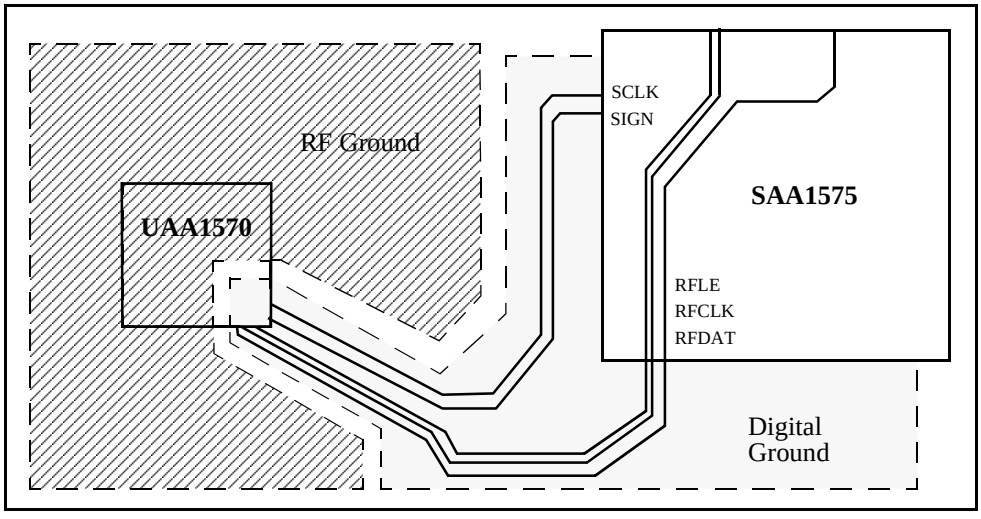


Figure 28 Digital Interface Routing Between SAA1575 and UAA1570

4.7 Clock Circuits for SAA1575

The suggestions made in this section are standard practice and not specific to the chip-set itself. Although the system clock at 30 MHz is probably far enough away from our first IF not too be problematic it is considered good practice to try and keep this circuit on the opposite side of the board to the UAA1570.

- The crystals should be kept close to the respective pins of the SAA1575.
- The circuit layout should be symmetrical so that any stray effects are common to both sides of the oscillator circuit.
- Ideally keep the 30 MHz crystal circuit well away from the RF layout, preferably on the opposite side of the board.
- Try to keep all ground returns from the loading capacitors as low impedance as possible back to the associated ground pins of the SAA1575.

5 GPS MOTHER-BOARD DESCRIPTION

This section provides design information for the mother-board of the EXACT low cost reference system. The main purpose of the mother-board is to provide regulated power supplies for the GPS engine as well as an RS232 interface to allow serial communication with a PC and RTCM-SC104 differential correction data to be received. Interfacing between the mother-board and GPS engine is via a 20 way header connector.

5.1 Power Supplies

The mother-board provides 4 power supplies for the GPS engine. The GPS system supply which consists of separate supplies for the RF and digital sections. A battery backup supply and a supply for an active GPS antenna. The antenna supply and system supplies are regulated from a 7 - 17 V supply input to 3 and 5 V. The main supply to the mother-board can be provided in two ways. Either from a low voltage, 2.1 mm, DC power socket (Centre terminal positively polarised), or from a 3 way molex connector (X5) with positive centre pin and negative each side. Both regulators have IN4002ID protection diodes to provide protection if supplies are connected in reverse. The IN4002ID diodes have a reverse voltage of 100 volts.

5.1.1 GPS System Supply

The GPS system supply is broken down into isolated RF and digital supplies. These are both at 3 volts and supplied by the same voltage regulator, U3. Figure 29 on Page 74 shows the voltage regulator circuit providing the 3 volt system supply.

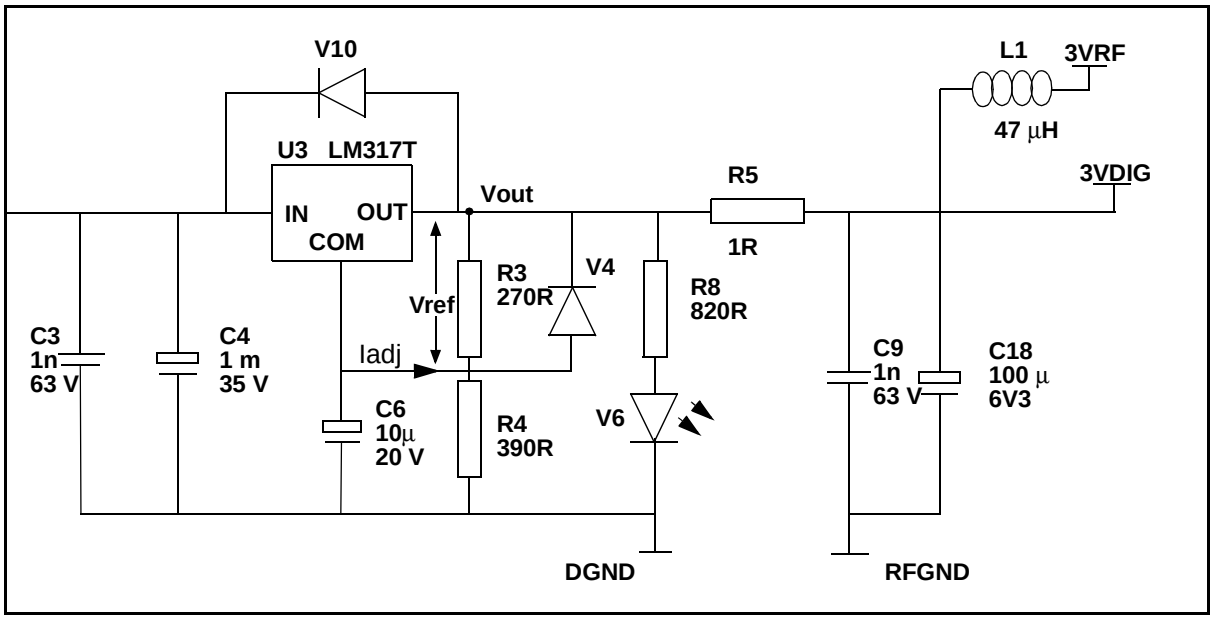


Figure 29 System Supply Voltage Regulator Circuit

The circuit around the LM317T 3 terminal floating regulator is a standard application taken from the data sheet for the device. The resistors R3 and R4 are used to set the output voltage, determined by the following equation:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{adj}R2$$

In this case, R2=R4=390R and R1=R3=270R. Vref is the voltage across R3 and is specified in the datasheet for the LM317T as 1.25 volts. The current Iadj is also specified as 50 µA. Using the values calculated for R3 and R4 we get Vout as 3.08 volts. This is designed on the high side of three volts to allow for some drop across R5 and inductor L1 in the RF supply path.

C4 is recommended in the application at 1 µF and C6 recommended as 10 µF. This should improve ripple rejection.

The diodes V4 and V10 are required to prevent the capacitors discharging through the regulator. D1 prevents C18 from discharging through the regulator during an input short circuit. D2 protects against capacitor C6 discharging through the regulator during an output short circuit.The combination of both diodes prevent C6 from discharging through the regulator during an input short circuit.

C9 and C3 shown in the circuit offer further supply decoupling and L1 offers further protection for the RF supply removing high frequency ripple.

The 1R resistor, R5, allows the system current to be monitored.

The 3 volt system supplies VRF and Vdig are provided to the system board on pins 2 and 20 respectively.

5.1.2 Battery Backup Supply

The battery backup supply for the system board is provided by the 3 volt Lithium cell, G1. This is switched in by switch S2, made available to the GPS engine on pin 3 of the header. In battery backup operation 12 μA is drawn from the battery. The 1 kOhm resistor R9 is in series with the battery to offer current limiting protection in the event of a short circuit, preventing damage to the lithium cell.

5.1.3 GPS Antenna Supply

The GPS antenna supply is provided on pin1 of the interface header. This can be switched between 0, 3 and 5 volts by switch S3. The 3 volts is supplied by the 3 VRF regulated supply and the 5 volt supply is provided by an identical LM317T application configured to provide a regulated supply of 5.09 V. An active antenna is expected to draw in the region of 25 mA with a 5 volt supply.

5.2 RS232 Interface

The RS232 circuit using the MAX562CWI IC is the standard application described in the datasheet for the device. This device has the capability of using 3 transmit and 5 receive lines. Only 2 of each are required in this application. The 3 V digital supply is used to supply the IC. This is a noisy part of the mother-board and it is essential it is isolated from the system supply. It must also be noted that this circuitry should be kept as far away from the GPS engine as possible. On the mother-board it is positioned on the opposite side of the board with the ground plane providing protection for the GPS engine.

The transmit and receive lines for the GPS engine are available on pins 11,12 of the header for Port0 and 14,15 for Port1.

The mother board has 2 male 9 pin D-type connectors to allow serial data to be passed to a PC. The D-type connectors are configured for use with a standard null modem cable to interface to a PC.

5.3 Master Reset Switch

The master reset switch (S1) is a push switch on the mother-board. This is connected to pin 5 of the interface header to the GPS engine. When pressed it pulls pin 5 to ground on the system board providing a manual over ride of the voltage detectors for PWR_FAIL and PWR_DN. Therefore pressing S1 pulls both lines low taking the baseband IC, SAA1575, into reset.

5.4 LED Indicators

There are 3 LED indicators on the mother-board. Two of these the yellow and green are the supply indicators. Each is in series with a 820R resistor to limit the current in the LEDs.

The third LED (red) is to show the 1PPS output form the GPS engine, which is available on header pin 19. This is supplied to the LED via a BJT inverter with a 47μ capacitor, increasing the effective pulse length of the signal. This delay makes the 1PPS output more visible to the user and provides a visual indicator that the receiver is tracking satellites.

6 SCHEMATICS AND BUILD STANDARDS

This section details the PCB's for the system. For both the Mother-board and GPS Engine the schematics, assembly drawings and detailed parts lists are provided. For the GPS Engine only the layout plots for all board layers are also provided for reference. Table 26, provides a list of cross references for all the PCB data provided in this section.

Table 26 Schematic and Build Standard Cross References

Description	Cross Reference
RF Schematic (GPS Engine)	Figure 30 on Page 77
Baseband Schematic (GPS Engine)	Figure 31 on Page 78
Mother-board Schematic	Figure 38 on Page 84
Assembly Drawings (GPS Engine)	Figure 32 on Page 79 & Figure 33 on Page 79
Assembly Drawings (Mother-board)	Figure 39 on Page 85 & Figure 40 on Page 85
Detailed Parts List (GPS Engine)	Section 6.4 on Page 82
Detailed Parts List (Mother-board)	Section 6.7 on Page 86
Layout Plots (GPS Engine)	Figure 34 on Page 80 to Figure 37 on Page 81

6.1 GPS Engine Schematics

The schematic for the GPS Engine is provided here in two sections for ease of reading. The first section is the RF Front-End design. This includes the UAA1570HL application and the reference clock circuitry. The Baseband Processor section includes the SAA1575HL application and associated RAM, ROM and reset circuitry.

Figure 30 GPS Schematic 1 RF Front-End

Figure 31 GPS Schematic 2 Baseband Processor

6.2 GPS Engine Assembly Drawing

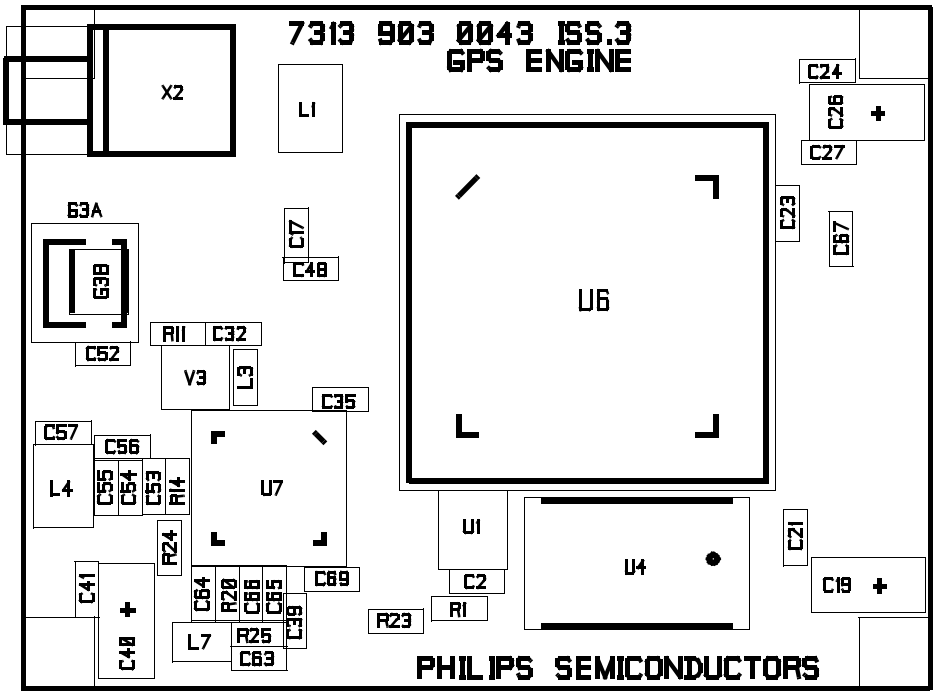


Figure 32 GPS Engine Component Ident (Top Layer)

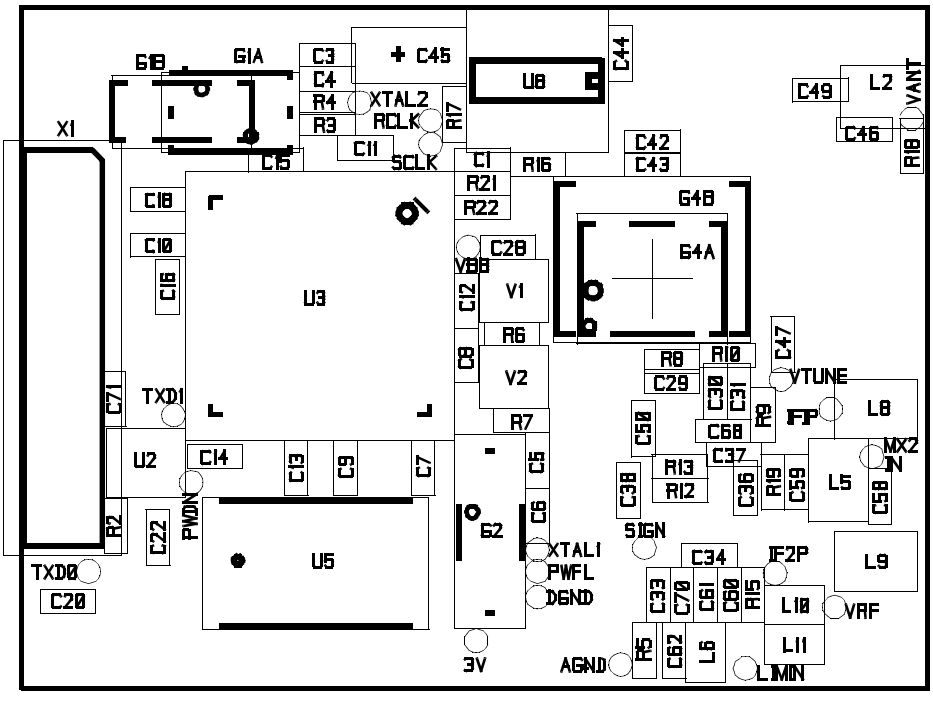


Figure 33 GPS Engine Component Ident (Bottom Layer)

6.3 GPS Engine Layout Plots

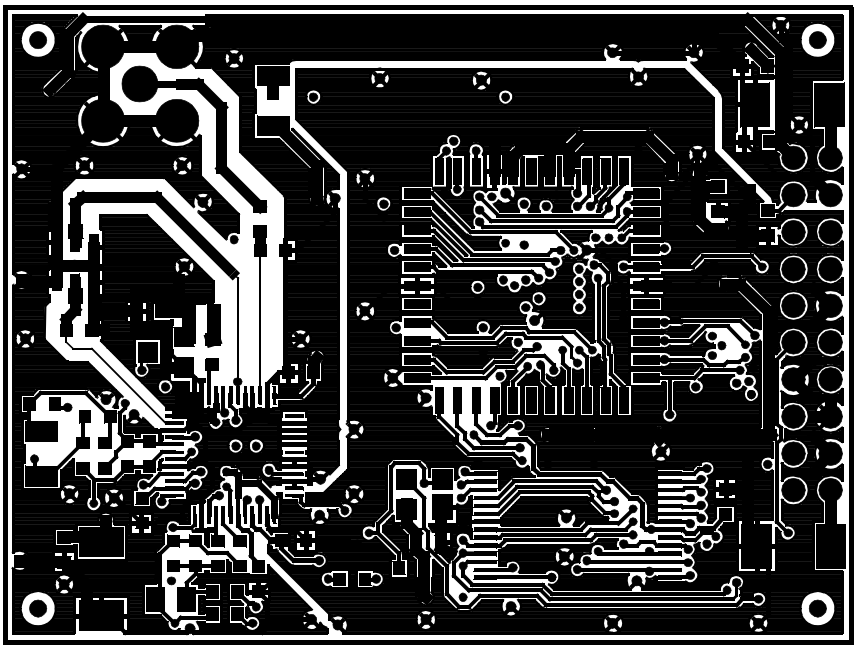


Figure 34 GPS Engine Layout (Top Layer)

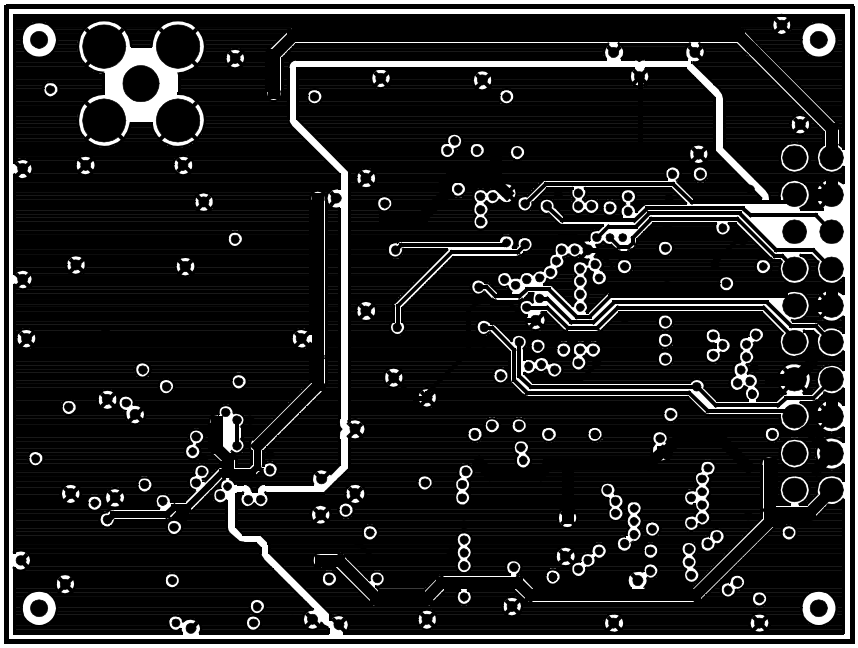


Figure 35 GPS Engine Layout (Inner Layer 1)

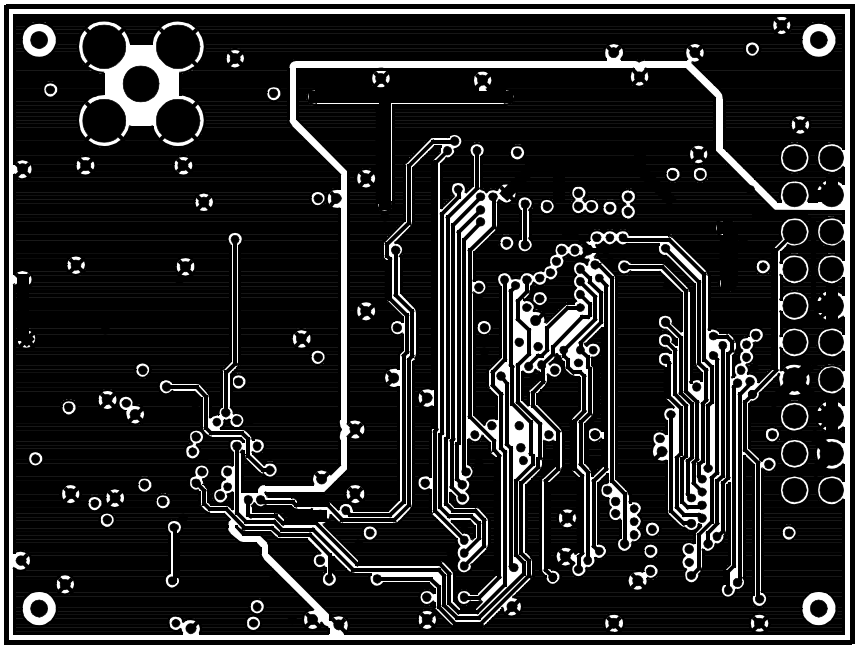


Figure 36 GPS Engine Layout (Inner Layer 2)

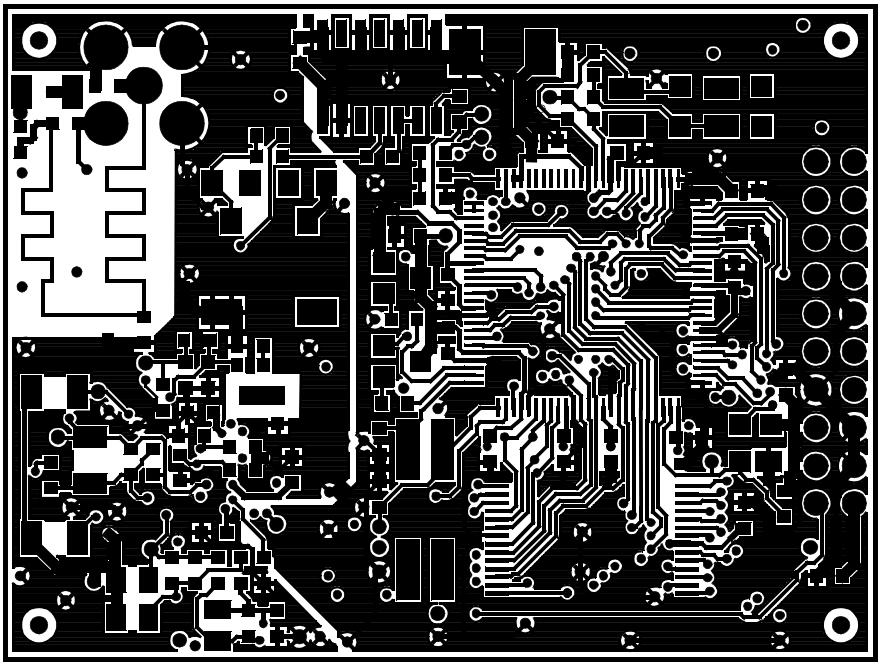


Figure 37 GPS Engine Layout (Bottom Layer)

6.4 Parts List For Gps Engine Board

Part Name/Number	Description	Quantity	Component
RESISTOR PHILIPS	RC-21(0603) Not Fitted	1	R23
RESISTOR BEYSCHLAG	FL_MMU0102-50BLF9090 MMU 0102	1	R19
RESISTOR PHILIPS	RC-21(0603) SM 100 k 5% 0.063W	2	R3, R16
RESISTOR PHILIPS	RC-21(0603) SM 100R 5% 0.063W	2	R4, R17
RESISTOR PHILIPS	RC-21(0603) SM 10 k 5% 0.063W	4	R1-2, R8, R11
RESISTOR PHILIPS	RC-21(0603) SM 10R 5% 0.063W	3	R12-13, R18
RESISTOR PHILIPS	RC-21(0603) SM 12 k 5% 0.063W	1	R14
RESISTOR PHILIPS	RC-21(0603) SM 1M 5% 0.063W	1	R7
RESISTOR PHILIPS	RC-21(0603) SM 2 k2 5% 0.063W	2	R15, R22
RESISTOR PHILIPS	RC-21(0603) SM 2 k7 5% 0.063W	2	R9-10
RESISTOR PHILIPS	RC-21(0603) SM 4 k7 5% 0.063W	2	R6, R21
RESISTOR PHILIPS	RC-21(0603) SM 820R 5% 0.063W	1	R20
RESISTOR PHILIPS	RC-21(0603) SM 0R	4	R5, R24-25, L11
CAPACITOR PHILIPS	0603 Not Fitted	3	C49-C50, C70
CAPACITOR PHILIPS	0603 SM 10n X7R	1	C29
CAPACITOR PHILIPS	0603 SM 10p NPO	1	C47
CAPACITOR PHILIPS	0603 SM 15p NPO	1	C32
CAPACITOR PHILIPS	0603 SM 18p NPO	2	C1, C62
CAPACITOR PHILIPS	0603 SM 1n X7R	2	C65-66
CAPACITOR PHILIPS	0603 SM 1p8 NPO	1	C48
CAPACITOR PHILIPS	0603 SM 2p0 NPO	1	C52
CAPACITOR PHILIPS	0603 SM 22n X7R	32	C2, C7-16 C18, C20-24 C27-28, C33-39 C41, C44 C67-69, C71
CAPACITOR PHILIPS	0603 SM 22p NPO	2	C3-C4
CAPACITOR PHILIPS	0603 SM 270p NPO	1	C30
CAPACITOR PHILIPS	0603 SM 27p NPO	1	C17, C5-C6
CAPACITOR PHILIPS	0603 SM 33n X7R	1	C46
CAPACITOR MURATA	0603 SM 36p COG MURATA GRM39 C	2	C53, C56
CAPACITOR PHILIPS	0603 SM 39p NPO	1	C59
CAPACITOR PHILIPS	0603 SM 47p NPO	2	C61, C63
CAPACITOR PHILIPS	0603 SM 4n7 X7R	2	C42-43
CAPACITOR PHILIPS	0603 SM 4p7 NPO	1	C31
CAPACITOR PHILIPS	0603 SM 68p NPO	1	C64
CAPACITOR PHILIPS	0603 SM 6p8 NPO	2	C54-55
CAPACITOR PHILIPS	0603 SM 82p NPO	1	C60
CAPACITOR PHILIPS	0603 SM 8p2 NPO	2	C57-58
CAP AVX-KYOCERA	TAJ(FAR_498-671) SM 22µ 10 V 10	2	C40, C45
CAP AVX-KYOCERA	TAJ(ES_401597AM) SM 22µ 6 V3 10	2	C19, C26

IC PHILIPS	74LVC04D(SO14) HEX INVERTER	1	U8
IC CYPRESS	CY62256VLL-70ZI 256 kBit SRAM (TSOP283)	1	U4
IC CYPRESS	CY62256VLL-70ZRI 256 kBit SRAM (TSOP283)	1	U5
IC PHILIPS	SAA1575(SOT407) GPS Baseband Processor	1	U3
IC PHILIPS	UAA1570(SOT313) RF Front-End Receiver	1	U7
IC SGS	M27W402 (PLCC44) 4MBit EPROM	1	U6
(Although in production it might be better to use a TSOP package part which are now more commonly available)			
IC MAXIM	MAX6315US26D3-T(SOT143) uP RES	1	U1
IC MAXIM	MAX6315US29D3-T(SOT143) uP RES	1	U2
Filter MURATA	DFC21R57P002HHC GIGAFIL 1.575G	1	G3A
OSC GOLLEDGE	GTXO-566T 14M4 Hz TCXO	1	G4B
CRYSTAL GOLLEDGE	GSX-1B 30M00 Hz SM Crystal	1	G1A
CRYSTAL SEIKO	MC406 32.768 kHz SM Watch Crystal	1	G2
DIODE ALPHA	SMV1233-004(SOT23) Var. Cap. Diode	1	V3
SM COMP PHILIPS	Si. Planar Epi. Tran. BC858B	2	V1-2
INDUCTOR Coilcraft	1008CS-181XJBC 180 nH 5%	2	L8-9
INDUCTOR Coilcraft	1008CS-331XJBC 330 nH 5%	2	L4-5
INDUCTOR MURATA	LQG11A5N6S00 5n6H SM	1	L3
INDUCTOR TOKO	FSLU2520-220J 22 µH 5% Inducto	2	L6-7
INDUCTOR TOKO	FSLU2520-270J 27 µH 5% Inducto	1	L10
INDUCTOR TOKO	FSLU2520-270J NOT FITTED	1	L11
INDUCTOR TDK	NLC322522T-150 k Inductor 15 µH	2	L1-2
CONNECTOR MOLEX	4030 kk HEADER 20-Way	1	X1
CONNECTOR IMS	ES_252-907055F SMA Skt Vertical	1	X2

6.5 Mother-Board Schematic

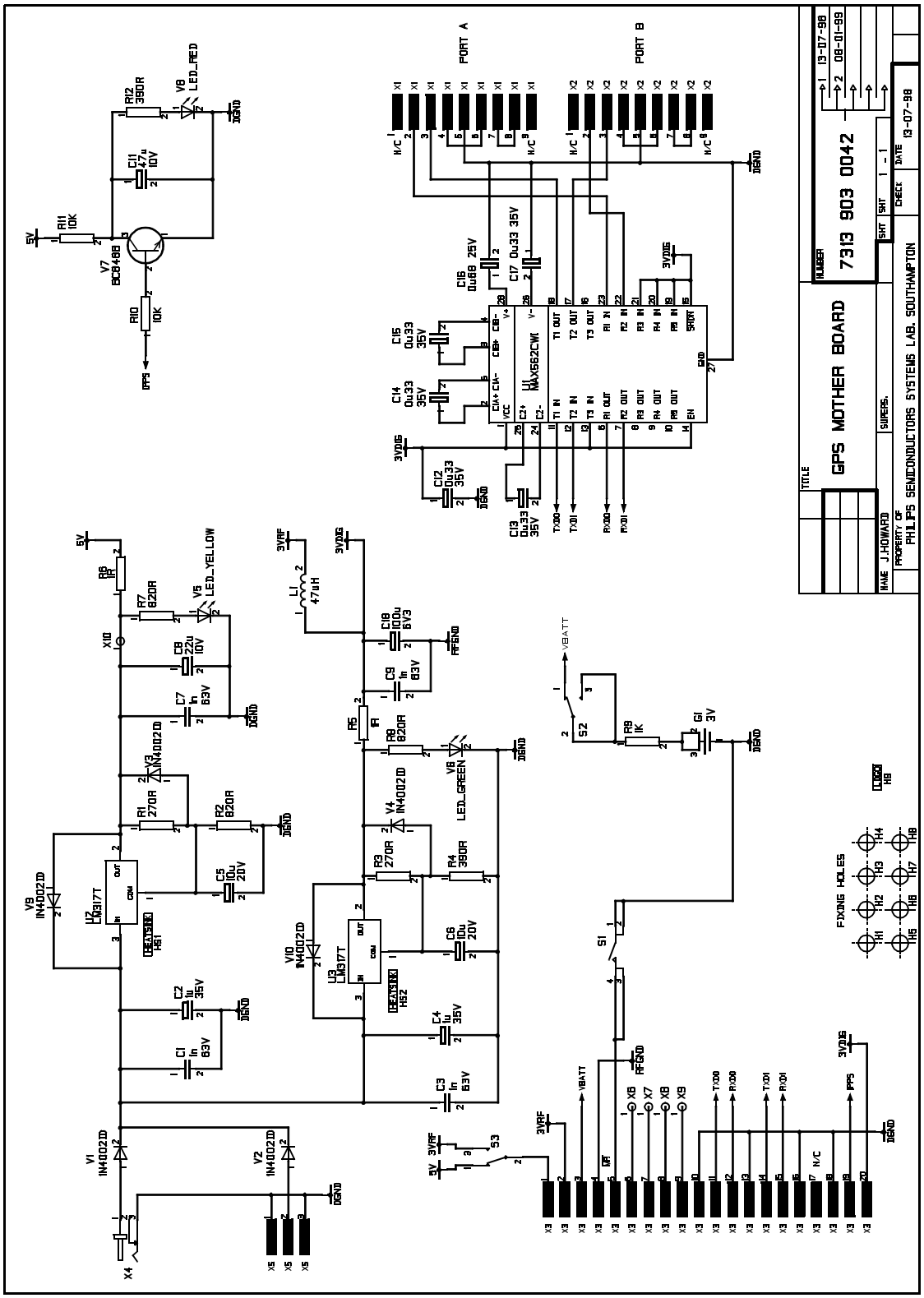


Figure 38 Schematic Diagram for GPS Mother-Board

6.6 Mother-Board Assembly Drawing

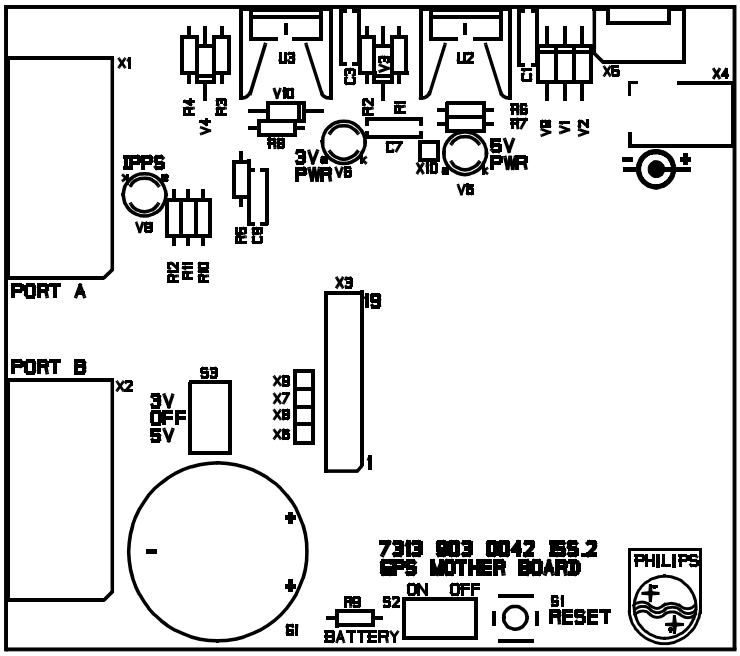


Figure 39 GPS Mother-Board Component Ident (Top Layer)

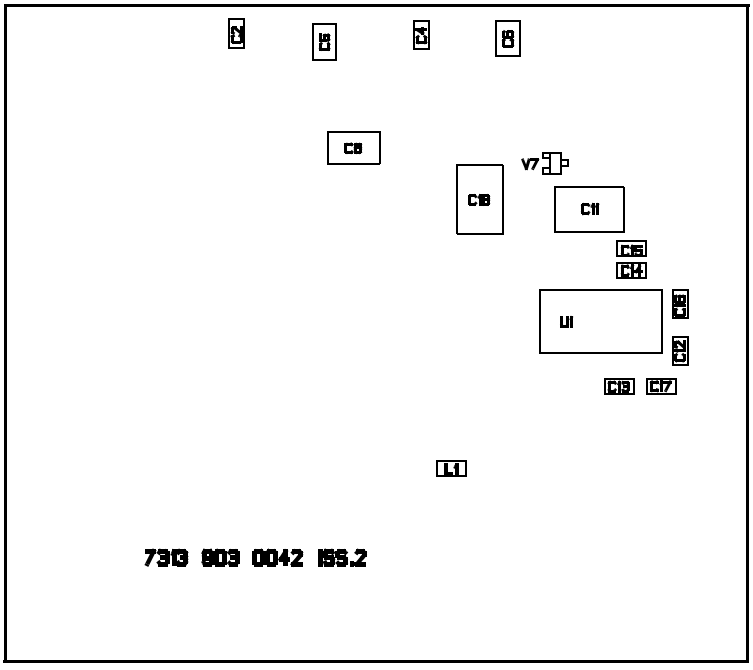


Figure 40 GPS Mother-Board Component Ident (Bottom Layer)

6.7 Parts List For Gps Mother-Board

Part Name/Number	Description	Quantity	Component
CAPACITOR PHILIPS	629 1n 63 V Minimum Ceramic Plate	4	C1, C3, C7, C9
CAP AVX-KYOCERA	TAJ SM 0u33 35 V 1	5	C12-15, C17
CAP AVX-KYOCERA	TAJ SM 0u68 25 V 1	1	C16
CAP. AVX-KYOCERA	TAJ SM 100µ 6 V3 1	1	C18
CAP AVX-KYOCERA	TAJ SM 1µ 35 V 10%	2	C2, C4
CAP AVX-KYOCERA	TAJ SM 22µ 10 V 10	1	C8
CAP AVX-KYOCERA	TAJ SM 10µ 20 V 10	2	C5-6
CAP. AVX-KYOCERA	TAJ SM 47µ 10 V 10	1	C11
RESISTOR PHILIPS	SFR16 10 k 5% 0.5W Metal Film	2	R10-11
RESISTOR PHILIPS	SFR16 1 k 5% 0.5W Metal Film	1	R9
RESISTOR PHILIPS	SFR16 1R 5% 0.5W Metal Film	2	R5-6
RESISTOR PHILIPS	SFR16 270R 5% 0.5W Metal Film	2	R1, R3
RESISTOR PHILIPS	SFR16 390R 5% 0.5W Metal Film	2	R4, R12
RESISTOR PHILIPS	SFR16 820R 5% 0.5W Metal Film	3	R2, R7-8
DIODE PHILIPS	Si. Diffused Rect. Diode 1N400	6	V1-4, V9-10
SM COMP PHILIPS	Si. Planar Epi. Tran. BC848B	1	V7
IC MAXIM	MAX562CWI(SO28) SERIAL INTERFA	1	U1
INDUCTOR	Inductor SM 47 µH 20%	1	L1
FIXING HOLE	Fixing Hole All Sizes	8	H1-8
HEATSINK REDPOINT	PF436 For TO220 2	2	HS1-2
REGULATOR	Adj. Volt. Reg. Pos. RS LM317T	2	U2-3
SEMICOND. PHILIPS	LED GREEN 5 mm Std. Diffused	1	V6
SEMICOND. PHILIPS	LED RED 5 mm Std. Diffused	1	V8
SEMICOND. PHILIPS	LED YELLOW 5mm Std. Diffused	1	V5
CONNECTOR ITT-CANNON	LV DC Power skt. 2	1	X4
CONNECTOR STOCKO	MKS3730 3 Way Connector	1	X5
CONNECTOR McMURDO	Plug 9 Way D Type	2	X1-2
TEST TERM. W.HUGES	Raised Loop Black	5	X6-10
CONNECTOR RS	SKT 20-WAY TOP ENT	1	X3
SWITCH APEM	SPDT ON-OFF-O Switch	1	S3
SWITCH APEM	SPDT ON-ON Switch	1	S2
SWITCH BOURNS	SPNO Sealed Switch	1	S1
BATTERY	3 V Lithium Cell	1	G1

7 TEST INSTRUCTIONS

This section provides a brief description of a sequence of tests that can be carried out to verify the functionality of the GPS system. All limits provided within these instructions are intended as proposals only and do not necessarily constitute part of the system specification.

7.1 Test Equipment Required

Table 27 provides a list of test equipment that is ideally required to carry out in depth PCB verification To establish basic functionality and performance some of the equipment may not be required.

Table 27 Test Equipment Description

TYPE	Equipment Description
Oscilloscope	HP54645D (2+16 Channels)
Spectrum Analyser	HP8594E (9 kHz to 2.9 GHz)
FET Probe	HP85024A (300 kHz to 3 GHz)
CW Signal Generator	Rohde and Schwarz SMH02 (100 kHz to 2 GHz)
PC	486 or better
GPS Simulator	GSS STR2760 (10 channels) or STR4760 (12 channels)
Multimeter	Fluke

7.2 DC Voltage Checks

This section outlines the main DC level checks required to verify, supply voltages, reset circuits, battery backup switching and VCO tuning.

7.2.1 System and Antenna Supplies

Measure the following DC system supply voltages:

Table 28 Test Instruction - DC Supply Voltages

Supply	Test Point	Spec Minimum	Spec Maximum	Typical
Digital	TP21	2.7 V	3.6 V	3.0 V
Vrf	TP8 (VRF)	2.7 V	3.6 V	3.0 V
* Vant (5 V) MEW VIC1	TP11 (VANT)	4.5 V	5.5 V	4.8 V
* Vant (3 V) SiGEM 3900	TP11 (VANT)	2.85 V	3.15 V	2.95 V

The antenna supply is dependent on that chosen on the mother-board with switch S3.

*The antenna supply should be measured with the antenna fitted. It is important to verify that the antenna supply is maintained within the manufacturers specified limits, normally 5% to 10%.

7.2.2 Battery Backup Supply, VBATT

- First check that the battery voltage is correct by measuring the voltage across the terminals of the battery on the mother-board.
- Switch S2 on the mother-board into the ON position to make the battery supply available to the GPS engine.
- Turn OFF the main power supply.
- Measure the battery backup supply on the GPS engine.

Table 29 Test Instructions - Battery Backup Supply

Supply	Test Point	Minimum	Maximum	Typical
VBATT	TP14	2.4 V	3.6 V	3.0 V

7.2.3 PWR_DN and PWR_Fail

If the main system supplies are correct, then PWRFAIL and PWRDN must be high to bring the baseband IC out of reset. The critical aspect to the power up and reset circuit is that the voltage monitor for PWR_DN is always higher than the specified threshold. For the Reference design a 2.9 V threshold has been chosen. It should also be verified that both PWR_FAIL and PWR_DN remain low for at least 1mS after the digital supply reaches 2.2 V. This can be done using a scope and triggering on the PWR_FAIL rising edge.

Table 30 Test Instructions - PWR_DN and PWR_FAIL

Signal	Test Point	Minimum	Maximum	Typical
PWRDN	TP6	2.95 V	3.15 V	3.0 V

7.2.4 VCO Tuning Voltage

The following DC checks provide a level of confidence in the functionality of the VCO circuitry. These measurements should be made using a scope and X10 probe to minimise loading effects on the circuit.

Table 31 Test Instructions - VCO Tuning Voltages

Signal	Test Point	Spec Minimum	Spec Maximum	Typical
VTUNE	TP12	0.2 V	2.4 V	0.9 V ± 20%
TANK	RF IC pin 10	1.822 V	2.011 V	1.92 V

7.3 System Power Consumption

The system power consumption is typically measured by removing the GPS engine from the mother-board and connecting supplies directly to the interface header of the GPS engine.

7.3.1 Normal Operation

To test in normal operation power up the digital and RF supplies for the GPS engine from separate 3 volt supplies and monitor the current for each supply.

Table 32 Test Instructions - Typical System Power Consumption

Supply	Header Connection	Maximum Current	Minimum Current	Typical
Digital	Pin20 3 V, Pin 18 GND	56 mA	50 mA	53 mA
RF	Pin2 3 V, Pin 4 GND	58 mA	52 mA	54 mA

7.3.2 Battery Backup mode

The power consumption in backup mode can be measured in the same way except providing power to the backup supply for the GPS engine.

Table 33 Test Instructions - Battery Backup Power Consumption

Supply	Header Connection	Maximum Current	Minimum Current	Typical
Vbatt	Pin3 3 V, Pin 13 GND	15 µA	10 µA	13 µA

7.4 VCO Phase Noise

This test looks at the Phase Noise performance of the VCO.

Terminate the SMA RF connector with a 50 Ohm load.

The output at IF1P (pin 17) is monitored using a spectrum analyser, with a X10 FET probe to minimise loading effects on the circuit. To gain reasonable results at this frequency it is essential that very short ground connections are made from the probe. Where this is not possible a better approach is to feed a CW signal at 1.57542 GHz into the RF connector at a level of -70 dBm. The same test can now be carried out but monitoring the 41.82 MHz IF output rather than the VCO feedthrough under no input conditions.

7.4.1 Inband Phase Noise up to 10 kHz

This test looks at noise in the passband of the PLL filter, which has a bandwidth of < 35 kHz. The spectrum analyser setup used for these measurements is given in Table 34:

Table 34 Test Instructions - In-Band Phase Noise Measurement Set-Up

Offset from Carrier	Centre Frequency	Span	Resolution Bandwidth
1 kHz	1.5336 GHz 41.82 MHz if Sig Gen Used	2 kHz	30 Hz
10 kHz	1.5336 Ghz 41.82 MHz if Sig Gen Used	20 kHz	100 Hz

a) Whilst monitoring the IF1P output at Pin 17, plot the output response using video averaging over approximately 10 samples.

b) Pause the analyser and hold the plot on the display.

c) Note the peak level at the centre frequency (1.5336 GHZ or 41.82 MHz).

d) Measure the noise floor in a 1 Hz bandwidth (dBm/Hz) at each offset.

e) The difference is the phase noise.

The phase noise results inband are:

Table 35 Test Instructions - In-Band Phase Noise

Offset	Peak (dBm)	Noise (dBm/Hz)	Phase Noise
1 kHz	-31	-101	-70 dBc/Hz
10 kHz	-31	-103	-72 dBc/Hz

7.4.2 Outband Phase Noise Up To 100 kHz Offset From Carrier

This test looks at the phase noise out of the band of the PLL filter up to 100 kHz offset. The test is carried out in exactly the same way as with the in-band tests described in Section 7.4.1 on Page 89.

The spectrum analyser setups are:

Table 36 Test Instructions - Out-band Phase Noise Measurement Set-Up

Offset from Carriert	Centre Frequency	Span	Resolution Bandwidth
20 kHz	1.5336 GHz	40 kHz	300 Hz
50 kHz	1.5336 GHz	200 kHz	1 kHz
80 kHz	1.5336 GHz	200 kHz	1 kHz
100 kHz	1.5336 GHz	200 kHz	1 kHz

The results expected are:

Table 37 Test Instructions - Out-Band Phase Noise

Offset	Peak (dBm)	Noise (dBm/Hz)	Phase Noise
20 kHz	-31	-105	-74 dBc/Hz
50 kHz	-31	-110	-79 dBc/Hz
80 kHz	-31	-113	-82 dBc/Hz
100 kHz	-31	-114	-83 dBc/Hz

7.5 SCLK Amplitude

Check that the reference clock is being divided down by the baseband IC and the amplitude of the signal. The sample clock, SCLK, is DC biased at approximately 1.5 V by the UAA1570.

Table 38 Test Instructions - SCLK Amplitude and DC Offset

Measurement @ Pin 37 (UAA1570)	Maximum	Minimum	Typical
DC Offset	1.50 V	1.48 V	1.49 V
Amplitude	700 mV p - p	400 mV p - p	500 mV p - p

The potential divider circuit reduces the SCLK input to the RF IC to keep it within a specified range. The levels provided in Table 38 are guidelines only, the absolute limits are detailed in Table 19 on Page 56. The nominal 500 mV level has been chosen to give plenty of headroom from the lower 20 mV limit and at the same time low enough to minimise any high frequency harmonics that may degrade the overall system performance without careful layout.

7.6 IF Filter Responses

Figure 16 on Page 41, and Figure 18 on Page 48 provide theoretical responses for the IF filters. This section explains how to measure the actual filter responses using a Spectrum analyser.

7.6.1 IF1 Filter Measurements

Spectrum analyser Setup:

Table 39 Test Instructions - IF1 Filter Measurement Set-Up

Centre Frequency	Span	Resolution Bandwidth
41.82 MHz	20 MHz	30 kHz

Procedure:

a) Feed a 1.57542 GHz signal at -70 dBm power into the RF connector of the GPS engine.

b) Probe pin22 (IF2INP) of the baseband IC with a X10 FET probe.

c) Use peak hold on the spectrum analyser to plot peak values for each frequency within the span.

d) Vary the input frequency to cover the span of the measurement effectively plotting the response of the filter itself. A step frequency of 10 kHz is recommended.

e) The resulting response should look similar to that given in Figure 41 on Page 92.

- -3 dB Bandwidth nominally 5 MHz.
- Peak output level at 41.82 MHz, nominally -35 dBm ± 10%.

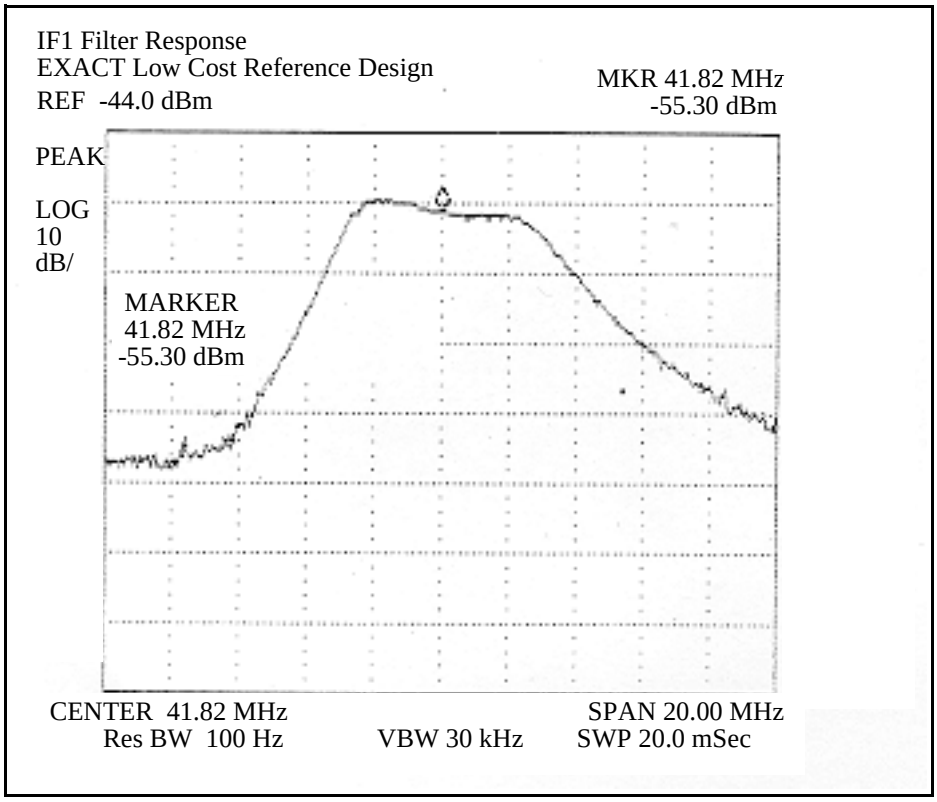


Figure 41 IF1 Filter Response

(This reading is a true reading. If using a X10 FET probe this will be measured at -55 dBm and must be corrected by 20 dBm to account for the X10 attenuation of the probe).

7.6.2 IF2 Filter Measurements

Spectrum analyser Setup:

Table 40 Test Instructions - IF2 Filter Measurement Set-up

Centre Frequency	Span	Resolution Bandwidth
3.48 MHz	6 MHz	30 kHz

Procedure:

a) Repeat the test for the IF1 filter except:

b) Probe pin 29 of the RF IC. This is the output of the second IF filter.

The measured filter response should look similar to that shown in Figure 42 on Page 93.

- -3 dB Bandwidth nominally 2.5 MHz.
- Peak output level at 3.48 MHz, nominally -10 dBm ± 10%.

(This is a true reading. If using a X10 FET probe this will be measured at nominally -30 dBm and must be corrected by 20 dBm to account for the X10 attenuation of the probe).

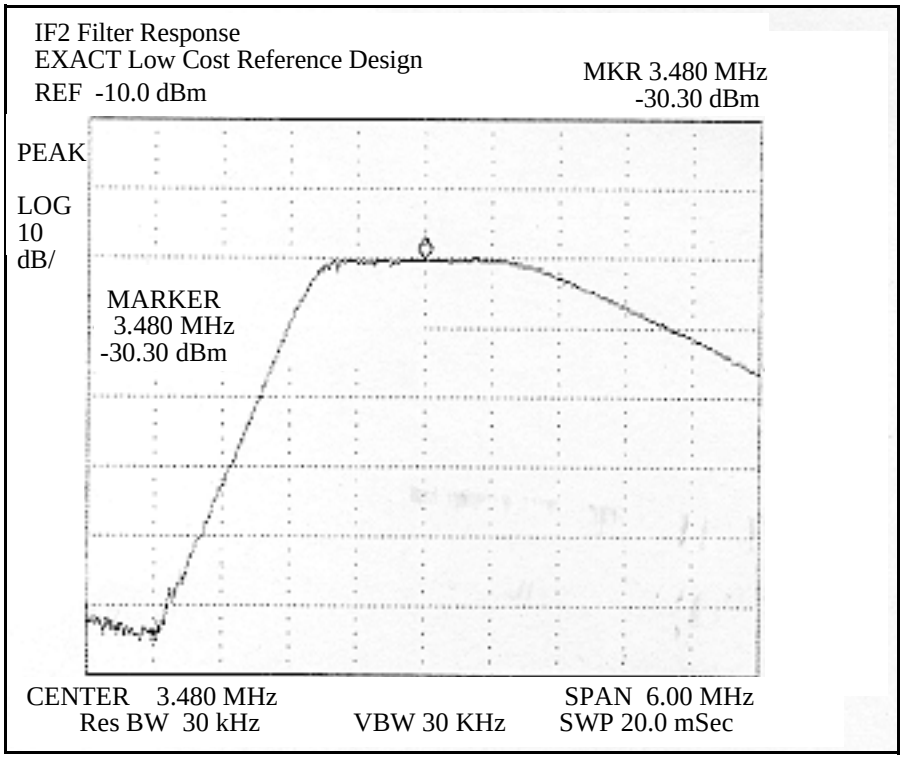


Figure 42 IF2 Filter Response

7.7 Gain Distribution

This test looks at the signal levels at various points around the RF front end. The results show the gains in the LNA and mixer stages and also the losses in the filters.

Feed a 1.57542 GHz C/W into the RF input connector on the GPS engine. Table 41 shows the points that should be probed along with the frequency of interest and that which the spectrum analyser should be centred at:

Table 41 Test Instructions - Gain Distribution

Measurement Point	Measurement Frequency	Typical Power (± 10%)
Pin 17 (IF1_P) mixer1	41.82 MHz	-30 dBm
Pin22 (IF2INP)	41.82 MHz	-35 dBm
Pin 24 (IF2P)	3.48 MHz	-10 dBm
Pin29 (LIMINP)	3.48 MHz	-11 dBm
PIN 34 (sign)	1.32 MHz	+10 dBm

(All readings given in Table 41 are true readings, ie: corrected from X10 FET probe measurements.)

Because it is so difficult to get reliable and accurate results at 1.5 GHz it is better to monitor the outputs at the IF stages. The output from Mixer1 can be taken as an indicator that adequate gain through good impedance matching has been achieved.

The typical benchmark measurements are the two mixer outputs and the SIGN output.

7.8 Sensitivity and System Noise Figure

There are two measures of sensitivity, that of the RF front end application and the other of the complete receiver. The receiver sensitivity is defined by the satellite signal level at which the receiver fails to provide a position fix. This can be measured using a GPS simulator, and slowly decereasing the satellite signal level from a maximum to the level at which the GPS position is lost. To do this an external LNA, with identical characteristics to that of the antenna to be used, must be fitted between the receiver and simulator.

Table 42 Test Instructions - Receiver Sensitivity

	Maximum	Minimum	Typical
Sensitivity	-136 dBm	-132 dBm	-134 dBm

The RF front end sensitivity measurement is referred to as the -3 dB sensitivity. This measurement defines the reduction in input level to reduce the output by 3 dB. To do this correctly the cable loss between the simulator and receiver must be carefully calibrated. This is nominally 0.5dB to 1dB for 0.5m of 50 Ohm coaxial cable. The test procedure is defined below.

a) Feed a 1.57542 GHz C/W into the RF input connector of the GPS engine.

b) Measure the maximum power at the SIGN output (pin 34).

c) Reduce the input signal until the SIGN output reduces by 3 dB.

d) The -3 dB sensitivity is given by the level of the signal generator plus calibrated loss of the cable used. **ie: -3 dB sensitivity = Meter Reading + Cable Loss**

It is possible to estimate the overall system Nose Figure by repeating the -3dB sensitivity test but with an external low noise amplifier included in the signal path. The amplifier chosen should be of known Noise Figure and exhibit a gain close to the upper limit for the system, in this case 25 dB with NF = 2 dB.

e) In this instance the estimated system Noise Figure is the difference between the two sensitivity readings plus the Noise Figure of the external LNA.

ie: Estimated System NF = {Sensitivity (Ext LNA) - Sensitivity (Without LNA)} + NF of LNA

The noise figure of the LNA used to produce the results below is 2 dB.

Table 43 Test Instructions - -3dB Sensitivity and Estimated Noise Figure

	Maximum	Minimum	Typical
-3dB Sensitivity (no LNA)	-104 dBm	-100 dBm	-102 dBm
-3dB Sensitivity (LNA)	-108 dBm	-107 dBm	-107.5 dBm
Noise figure	8 dB	5 dB	7.4 dB

7.9 Functional Performance

The tests in this section should only be carried out when the previous tests have been completed and the system seems to be functioning correctly.

7.9.1 Position Accuracy

To test the position accuracy, the receiver should be situated in an open site condition, ie: with a clear view of the sky. The system should be used with an active antenna with around 25 dB of gain. The system should also be connected to the serial input of a PC running the Host software, to enable position data to be logged.

The critical aspect of this test is the precise position of the receivers antenna at the time of the test. Typically this would be carried out using a GPS simulator and can therefore be specified by the user. However, in the absence of such equipment the engineer must be able to accurately determine the antenna position at the time of test by other means.

Procedure:

a) Allow the system to obtain a valid position fix.

b) Log the GGA NMEA messages for a minimum of 12 hours. (Refer to Quick Start Guide in Reference [3].

c) Post process the NMEA messages, comparing the positions given by the receiver to the known location of the antenna at the time of test.

The results for the test should be within the following specification:

Table 44 Test Instructions - Standard Horizontal Position Accuracy (95%)

	Horizontal
Specification	100 m
Typical	58 m

7.9.2 Satellite Signal Level

This test makes a check that the carrier to noise ratio of the satellite signals is high enough. A low SNR could indicate that there is a problem with the system.

A quick test is to look at the SNR fields in the GSV NMEA messages when the system is set up as in Section 7.9.1. Normally SNRs of 50 - 52 dB are seen the for highest elevated satellites under open site conditions using a 25 dB active antenna.

A more detailed test requires the use of a satellite simulator. The signal input level can be varied and the SNR levels noted for the highest elevated satellites. Table 45 shows typical results:

Table 45 Test Instructions - Satellite SNR Level Sensitivity

Satellite Power (Relative to STANAG Minimum)	SNR
+20 dB	52
+15 dB	47
+10 dB	42
+ 5 dB	37

7.9.3 Acquisition Time (TTFF)

The acquisition test requires the same set-up as in Section 7.9.1 on Page 95. Similarly open site test conditions are critical when measuring the performance against the system specification. A provision is made within the PC Host software to simplify this test procedure. (See Reference [3]). The Receiver Status Window, contains three acquisition modes, Hot, Warm and Cold start. If any of these is pressed the receiver is reset into an acquisition state and a timer started. The timer stops upon receipt of a valid NMEA position message and as such provides a TTFF.

This test is best carried out by allowing the receiver to establish a position fix and then download a full almanac and ephemeris database, which can take up to 15 minutes. The acquisition tests can then be carried out in the following order.

HOT START

The HOT start procedure resets the receiver without disturbing any of the data held by the receiver. The timer is initiated and stopped upon receipt of the first valid position fix.

WARM START

The WARM start procedure resets the receiver and invalidates the receivers ephemeris data. This test is similar to the receiver being left off overnight, where almanac data, time and last known position are still valid. As with the HOT start test a timer is initiated at the start of the test and held upon receipt of the first valid position output.

COLD START

The COLD start procedure resets the receiver and invalidates all receiver data. This test is similar to a receiver being powered on for the very first time with no aiding data available to it. Similar to the HOT and WARM start tests a timer is initiated at the start of the test and held upon receipt of the first valid position output.

Table 46 Test Instructions - Acquisition Times (TTFF)

Acquisition Mode	Maximum	Minimum	Typical
COLD	< 500 secs	60 secs	< 120 secs
WARM	50 secs	40 secs	45 secs
HOT	12 secs	8 secs	10 secs

Typical results for these tests are shown in Table 46. The results for WARM and HOT starts must be obtained after the receiver has had enough time to retrieve all almanac and ephemeris data.

7.9.4 Reacquisition Time

Time

The reacquisition time is the time taken for a position to be obtained after all satellites have been made invisible to the receiver.

The simplest way of carrying out this test is to turn off the active antenna supply on the mother-board for the required time and then time how long it takes to obtain a position fix when the power is re-applied. It is best to repeat the test to get an average.

A more sophisticated method requires a satellite simulator. The power received from the satellites can by reduced to zero for periods of time and then re-applied. The simulator can be programmed to do this a number of times to allow an average reacquisition time for a specific outage time to be obtained.

Typical results for the test are shown in Table 47.

Table 47 Test Instructions - Reacquisition Time

Obscuration Time	Maximum	Minimum	Typical
10 secs	2 secs	1 sec	1 sec
60 secs	3 secs	1 sec	2 secs
600 secs	15 secs	3 secs	6 secs

7.9.5 Serial Communication

A quick check of the serial communication can be carried out by first connecting Serial Port'A' of the system to a PC running the Host Software using a standard null modem serial lead. Any command can then be sent to verify the two way communication process such as enable all NMEA messages.

ie: $PHILS,NME,ALL,A,ON

This message can be sent from the 'Edit NMEA Messages WIndow'. The "Incoming NMEA Messages" window should then display all NMEA messages supported by the receiver scrolling up the screen.

Port 'B' can now be tested in the same way to verify the two way communication interface. It should be noted that these tests only check the receiver at its default baud rate of 4800. If all possible baud rates are to be tested this would have to be done using a terminal emulator accessory on the PC or some other means developed by the user.

The command $PHILS,SPD,A,<speed> can be used to set the baud rates of the ports and is described in Section 4 of Reference [3].

7.9.6 Differential GPS

These tests are aimed at both verifying DGPS functionality as well as DGPS position accuracy. To do this a source of valid RTCM correction data must be provided to the receiver under test. This would normally take the form of an RDS receiver or similar receiving encrypted correction data and outputing the corresponding RTCM correction data on its serial port. DGPS mode can be set up as follows.

Connect serial port A to a PC running the PC Host software.

Connect Port B to a suitable DGPS receiver outputing RTCM-SC104 correction data.

Issue the following commands using Port 'A':

$PHILS,RTC,AUT,N	This forces the receiver into a DGPS output only
$PHILS,SPD,B,<baudrate number>	Sets the Port 'B' baud rate to match the RTCM input
$ PHILS,RTC,MEM,B	Assigns RTCM input to Port 'B'

This will set up the receiver to receive RTCM data on port B at the specified baudrate. In this mode, only differentially corrected positions will be output by the receiver. A secondary method of verifying a differentially corrected output is to monitor the 6th field of the GGA message. This will be '1' for a standard positioning output and '2' for differentially corrected position outputs. Please refer to Reference [3] Section 4.3.

DGPS position accuracy can now be measured using the same test procedure outlined in Section 7.9.1 on Page 95.

The results for the test should be within the following specification.

Table 48 Test Instructions - DGPS Position Accuracy (95%)

	Horizontal
Specification	10 m
Typical	6 m

7.9.7 1PPS Output

A quick check that 1PPS is working is to observe 1PPS led on the mother-board when the receiver is outputing valid position data. The 1PPS output is enabled when at least one satellite is being tracked. The waveform can be observed with an oscilloscope on pin19 of the interface header. The waveform has a period of 1 second and a pulse duration of 1 ms.

Functionality can be quickly verified by waiting for the receiver to obtain a valid position fix and checking the 1PPS output is enabled. If the antenna is now removed or the power disabled from the mother-board, the 1PPS will be disabled and only enabled once the antenna is reinstated and at least one satellite is being tracked by the receiver.

8 TROUBLE SHOOTING GUIDE

Table 49 highlights a number of possible problems that may be encountered in early development together with a list of possible causes. Obvious problems such as misplaced or even missing components are not covered here rather issues that may result from either layout or design problems. Table 49 provides a brief guide with further explanations and references provided later in the section pointed to by the column, REF.

Table 49 Trouble Shooting Guide

REF	Fault Description	Possible Causes
8.1	VCO not running	1. Poor GND return structure for Varactor 2. Long trace lengths therefore reduce 'L'
8.2	Poor VCO Phase Noise	1. Poor Layout 2. Supply Decoupling 3. Loop Filter Components
8.3	Poor sensitivity	1. Self Jamming from Ref Clock 3rd Harmonics 2. Poor RF Matching Limiting Front End Gain 3. IF Filter Response Poor (Mistuffed Components?) 4. SAW or Ceramic BPF inadequately grounded (High Loss)
8.4	No NMEA message output from SAA1575.	1. Failure to reset correctly 2. System Clock not running 3. No RCLK input to SAA1575
8.5	Failure to lock to satellites	1. Inadequate gain in system usually a result of mismatch 2. Instability due to active antenna close to PCB 3. Antenna view obscured partially or fully
8.6	Excessive Time To First Fix	1. Inadequate gain in system usually a result of mismatch 2. Poor satellite distribution limiting DOP ratio 3. Antenna view obscured partially or fully 4. Bad data stored in memory usually last valid position data 5. Battery backup circuit failure
8.7	Intermittent Power Up Failure	1. Borderline reset behaviour due to PWR_FAIL and PWR_DN control 2. RSTIME low restricting stabilisation time of system clock

Each of the possible causes listed in Table 49 are discussed in the following sections describing how the fault may occur and how the problem may be resolved.

8.1 VCO Not Running

The most common reason for failure in the VCO circuit is layout. The reference design has been chosen to run with a nominal 5.6 nH inductor in series with the varactor, SMV1233-004. If the trace lengths from Pin 10 up to the varactor are not kept as short as possible and reasonably clear of other components excessive stray effects can result. This ultimately increases the effect track inductance and results in a lower physical value for L being required.

A simple solution for excessive stray inductance is to reduce the physical inductor nominally from 5.6 nH to 3.9 nH. A symptom of this failure is that the tune voltage at Pin 40 will be high at approximately 2.4 V suggesting a need for lower tuning inductor.

However if vias have been used in this tuning path it is more than likely that physical inductor values of less than 3.9 nH are required and at this point tolerance effects in production may become an issue. For this reason it is very important that vias are not used in the tuning circuit for the VCO and the layout is as compact as possible with very short low impedance ground connection between the varactor ground and Pin 11 of the UAA1570. Ideally ground via(s) should be added to improve the low impedance return path for the VCO currents. See Section 4.3 on Page 68 on VCO layout guidelines.

8.2 Poor VCO Phase Noise Response

In order to maintain Phase Noise response it is critical that the layout of loop filter minimises the likelihood of local digital interference. The most likely cause of inband phase noise, ie: within 20 kHz, will be low frequency digital noise due to either supply line routing or close proximity real time clock circuit. It is important to keep the real time clock crystal circuit well away from the loop filter components. If this is not possible move the loop filter closer to the VCO circuit. Refer to Section 4.3 on Page 68 on VCO layout guidelines.

Another source of interference can be ground loops in the supplies. Ideally the power connector should be positioned in the middle of the board with the supplies splitting off independently to the RF and digital sections. The supplies in each path should branch off from one path avoiding looping the supply in a circular fashion around each section.

The choice of loop filter components will effect the overall phase noise response. It is recommended for the default application that a 10 k and 10 n series combination is used in parallel with 270 pF. This gives about a 35 kHz bandwidth and produces a non peaky response. Refer to Section 3.3 on Page 34 on VCO application.

8.3 Poor Receiver Sensitivity

There are three main reasons for poor receiver sensitivity. Inadequate gain in the RF stages of the design, either through impedance mismatch or poor grounding of the ceramic filter. Self jamming in the IF stages as a result of poor reference clock layout. Poor IF filter response most likely as a result of misplaced components.

The gain can be verified easily by feeding in an external CW signal at 1.575 GHz at around -70 dBm whilst monitoring the first mixer output at Pin 17. This value should be nominally -30 dBm in a single LNA application. If this is more than 3 dBm lower then it is likely that optimum transfer gain has not been achieved. In this case the matching would need to be verified.

Measuring the IF filter responses is covered in Section 7.6 on Page 91, making it easy to identify any problems here. The design used on the reference system is very well established and any problems here will more than likely be a result of misplaced components in manufacture.

The problem of self jamming can be verified by looking at the SIGN output, Pin 34 with no external input to the receiver.The 14.4 MHz reference clock has a 3rd harmonic in the first IF passband. If mixed down further we can actually monitor its effect looking at the SIGN output around 60 kHz. If this 60 kHz peak is monitored over a nominal 10 kHz span and averaged we can measure what is referred to as jammer to Noise ratio.

Test Procedure:

- Measure the 60 kHz peak level and note it.(Typically +5 dBm).
- Measure the noise floor at nominally 62 kHz, in dB m/Hz (Typically -55 dBm/Hz).

We want to see how far below our integrated signal bandwidth the interfering 60 kHz spur is, which is done by converting the -55 dBm/Hz into our nominal 2 MHz signal bandwidth.

ie: 10 Log10 2 MHz = 63 dB Therefore -55 dBm/Hz approximates to +8 dBm (in a 2 MHz BW).

Therefore in this case our jammer is approximately 3 dB below our integrated signal bandwidth giving a Jammer to Noise Ratio of -3 dB.

As a guideline we can estimate that this jammer must be at least 13 dB below our integrated signal bandwidth to have less than 0.2 dB degradation on our system sensitivity. Once external gain is added via the antenna this J/N ratio will improve to nominally -15 dB to -20 dB and is never a serious issue in this case. However if the layout is not ideal this 60 kHz spur will be much higher and inevitably cause problems. As a guideline if the J/N is positive without an external amplifier connected the problem will almost certainly have to be addressed. Refer to Section 4.5 on Page 70 on Reference Oscillator layout guidelines.

8.4 No NMEA Message Output from SAA1575

The first thing to check in this case is that the IC is reset correctly and that the clocks are running. The reference clock from the RF IC, RCLK, must be present for the baseband to output NMEA messages. If this is not present the firmware detects a problem and prevents serial communications.

The system clock should normally run without any difficulty. It is important that a load capacitance rating for the crystal no greater than 20 pF is implemented with nominal 22 pF load capacitors. If this is not done the oscillator transconductance characteristics may be breached.

If the oscillator is running but no output is achieved it will normally be due to reset failure. The obvious problem may be that RSTIME is held low instead of high giving inadequate settling time for the oscillator otherwise it will be due to the PWR_DN and PWR_FAIL procedure.

PWR_FAIL and PWR_DN must be held low until after the SAA1575 supplies have gone above the nominal threshold level of 0.7 Vcc. A minimum delay of 1mS is recommended for this event to guarantee reset control. The rest failure can be easily detected by looking at the sample clock output SCLK, from the SAA1575. If the SAA1575 has not reset correctly the SCLK will be at 14.4 MHz instead of 4.8 MHz.

Please refer to the power up and reset design guidelines in Section 3.10 on Page 61.

8.5 Failure to Track Satellites

This fault can be caused by inadequate system gain, antenna obscuration or instability resulting from antenna being in close proximity to the board. Verifying the gain in the RF stages is covered earlier in this section.

If the antenna is not given a full view of the sky it will greatly reduce the system performance. At power up the receiver will use a look up table and or almanac data if present to search for satellites. If the chosen satellites are obscured it will not be able to acquire them. This may result in lengthy delays in acquiring satellites especially under Cold Start conditions. Therefore it may be a case of waiting to allow the receiver to find those that are visible. Another problem would be seen hanging the receiver out of a window. In this case the antenna is partially obscured and those satellites that are in view are likely to be severely affected by multipath signals reflected from the window itself. This again may greatly delay the acquisition or in worst cases prevent it.

Another possible cause of this may be if the antenna is in close proximity to the board itself. The antenna has relatively high gain at 26 dB and if too close to the board will pick up the RF signal from the board and lead to regenerative feedback. This can often be seen on a spectrum analyser by looking at the IF output at 40 MHz over a nominal 60 MHz span with the antenna attached. The noise floor can be seen to shift erratically as the antenna is brought close to the board. In a final design the RF stages would normally be shielded and the antenna intended to be some distance away ie: on the roof of the car.

8.6 Excessive Time To First Fix or No Valid Position Output

There are a number of issues that can affect Time To First Fix, TTFF. The most obvious ones are where the satellite distribution is poor or the antenna is being obscured. In both these cases the few satellites that are visible to the antenna result in poor satellite geometry and yield DOP levels outside the default mask settings of the receiver. PDOP is the Position Dilution Of Precision and is a figure of merit given to the geometry of the available satellites. Essentially the lower this figure the more accurate your position output is likely to be. The receiver defaults to a PDOP of 6 which ensures the standard 100m GPS accuracy is guaranteed for 95% of results. However under severe conditions this mask setting could be increased to compensate for poor conditions and allow the receiver to output valid data. As a guideline with the PDOP mask set at 12 it is likely that position outputs could actually move out as far as 200m in error. The benefit however is that you greatly improve the likelihood of valid output under critical conditions and once other satellites come into view so the DOP levels will fall and accuracy improve.

Another problem that could lead to acquisition problems is where the system gain is too low either through matching or poor filter design for example. The EXACT system has a default satellite signal level threshold of 37. If this level, as output in the NMEA message ‘GSV’, is lower than 37 the receiver will stop tracking it. In order to guarantee satellite acquisition this level ideally should be above 40. Under nominal conditions you would expect this level to fall between 48 and 52. If the satellite levels are as low as 42 to 40 it is likely that the receiver yields slightly longer TTFF performance. This can normally be caused by heavy foliage conditions such as overhanging trees or may point to poor RF matching at the front-end of the system. This can be determined easily by testing the system in good open site conditions and verifying a satellite level of nominally 50. (This assumes an EXACT reference design with a 26 dB active GPS antenna).

Another common problem is where the backed up data is invalid, ie: where the last valid position is greater than 500 km in error because the receiver has been moved. If this is likely to be the case then the receiver should be reset using the, $PHILS,INI command as described in Reference [3].

8.7 Intermittent Power Failure

If the oscillator is running but no output is achieved it will normally be due to reset failure. The obvious problem may be that RSTIME is held low instead of high giving inadequate settling time for the oscillator.

If this is not the case then the problem is most likely to be due to incorrect PWR_DN and PWR_FAIL procedure. PWR_FAIL and PWR_DN must be held low until after the SAA1575 supplies have gone above the nominal threshold level of 0.7 Vcc. A minimum delay of 1mS is recommended for this event to guarantee reset control. The rest failure can be easily detected by looking at the sample clock output SCLK, from the SAA1575. If the SAA1575 has not reset correctly the SCLK will be at 14.4 MHz instead of 4.8 MHz.

Please refer to the power up and reset design guidelines in Section 3.10 on Page 61.

9 MANUFACTURER DETAILS AND USEFUL URL'S

This section provides information and data on various components used in the EXACT Low Cost Reference Design. It is aimed at guiding the designer quickly to sources of information related to the receiver as well as provide guidelines on second sourcing of parts. Where applicable some information is provided on the benefits and drawbacks of using certain parts in the design with a view to cost and performance.

9.1 Integrated Circuits

This section covers the key peripheral components, such as RAM, ROM, voltage monitors and logic gates.

9.1.1 EPROM

The EXACT solution requires external program memory which meets the specification outlined in Table 50.

Table 50 Key EPROM Requirements

Parameter	Rating
Supply Voltage	3 V ± 5%
Capacity	2 MBit (128 k x 16)
Access Times	100 nS (Maximum)

In the reference design an SGS Thomson part has been used, which is a 44 pin PLCC part,

Part No: SGS Thomson M27W402-100 k6.

This is the only suitable 3 V PLCC part that we are currently aware of and there is no guarantee that this will remain in production for any length of time. It is suggested that any new design should implement a more commonly available part, the most common of which appears to be a FLASH device in a 48 pin TSOP package such as the SGS part M29W200B series. The M27W402 data can be found at the following website listed under OTP and UV EPROM products.

Website: http://www.two.st.com/stonline/products/selector/index.htm

9.1.2 SRAM

The EXACT solution requires external SRAM to be used. In the reference design Cypress parts have been used, this decision being based at the time on the lowest available cost price for a what is a fairly standard device. The SRAM chosen came in standard pinout and reversed pinout which greatly reduces PCB layout effort.

Part No: Cypress CY62256VLL-70ZI and CY62256VLL-70ZRI

Website: http://www.cypress.com/cypress/prodgate/sram/cy62256v.html

The data sheets for the SRAM used on the reference design can be found at the above website. The SRAM is again a fairly standard item, but the key specification parameters are highlighted in Table 51.

Table 51 Key SRAM Requirements

Parameter	Rating
Supply Voltage	3 V ± 5%
Capacity	256 kBit (32 k x 8)
Access Times	100 nS (Maximum)

9.1.3 Voltage Monitor ICs

The reset function for the SAA1575HL relies on the appropriate control of two reset pins on the IC. In the 3 V application described in this guide, the reset is controlled by two voltage monitor IC's which toggle the rest pins, PWR_DN and PWR_FAIL at given system supply levels. The behaviour is described in detail in Section 3.10 on Page 61.

There are a wide range of microprocessor supervisory ICs available on the market and the parts used in the reference design were selected primarily for low cost at the time of the design. The other useful feature of these parts was the option of a master rest function that could be used by a host system to reset the receiver under software control should this be a requirement.

Part No: Maxim MAX6315US26D3-T (2.6 V)
MAX6315US29D3-T (2.9 V)

Website: http://www.maxim-ic.com/Datasheets.htm

The choice of device is not highly critical and the choice is more likely to be driven by cost. The important factor in this design is that the functional requirements as specified in Section 3.10 on Page 61. are adhered to.

9.1.4 Reference Clock Squaring Circuit

The 14.40 MHz reference clock must be squared up prior to input to the SAA1575. To do this a simple two stage CMOS inverter has been implemented specifically on grounds of cost. The only possible drawback of this choice is the size of the package used, SO14, 74LVC04D.

Logic gates are now available in smaller outline packages such as the Toshiba TC range of components. In this case the TC7W04F could be implemented to replace the 74LVC04D in this application. The data sheet for the TC series logic from Toshiba can be found at the following website, if a search is entered for 'TC7W04F"

http://www.toshiba.com/taec/

9.2 Discrete Components

This section provides details of all discrete parts used in the low cost reference design including possible alternatives.

9.2.1 Varactors

The reference design implemented a double series varactor diode part, SMV1233-004, in order to maximise VCO gain and resonator Q, as well as the realisable inductor values used in the circuit. Data on this alpha part can be found at the following website and selecting varactors.

http://www.alphaind.com/advscripts/products/product/product.asp

An alternative replacement for the varactor part is from M/A-COM, MA4ST250CK-287. This is an identical SOT-23 package part with almost identical reversed biased capacitance at Ct = 1 V. The data for this part can be found at the following website, listed under silicon tuning varactors, High Q.

http://www.macom.com/products/prod_semi_diodes_tuning_siliSMT.asp

9.3 TCXO's and Crystals

The main driving force behind the choice of crystals and reference oscillator was to minimise cost without impairing performance. This section provides information on the parts used in the design and where possible suitable alternatives.

9.3.1 14.40 MHz TCXO's

The main selection criteria for the reference clock was,

- low phase noise -130 dBm/Hz at 100 Hz offset
- clipped sinewave output Typically 1 V p - p output
- Frequency tolerance and ageing ± 15 ppm over lifetime.

The Golledge part was the most competitively priced oscillator available to us at the time of the design, and is therefore the one specified in the parts list. All results undertaken with this device have been good. The data for the GTXO-566 range cab be found at the following website.

http://www.golledge.com/ Under (VC)TCXO's

Part No: GTXO-566T 14.40 MHz.

The footprint for the Golledge oscillator was identical to the RAKON range of TCXO's. The IT225BE is anticipated to be slightly more expensive than the Golledge part but may provide better stability in terms of shock and vibration performance. RAKON have a history of supplying for the GPS market and as such have tailored their manufacturing and testing to provide improvements to temperature behaviour, G sensitivity and phase noise performance. The only drawback to this is that potentially they are not the cheapest option. The data for the IT225 range can be found at the following website.

http://www.rakon.com/models/oscillator-search Under SMD TCXO's and VCTCXO's

Part No: IT225BE 14.40 MHz

9.3.2 30 MHz Crystals (Processor Clock)

The 30 MHz crystal was really a standard item, but the main concern was to minimise the cost and therefore the Golledge part is the one specified in the parts list. However a wide range of alternatives are available provided the following specification points are considered.

- MUST be a fundamental crystal
- Frequency tolerance nominally < ± 100 ppm
- Load Capacitance < 20 pF (Typically 16 pF to 20 pF).

The Golledge part used on the reference design was the GSX-1B 30.00 MHz, and the data can be found at the website given Section 9.3.1 on Page 105 in. Possible alternative parts can be found from, IQD and ACT as detailed below:

http://www.iqdcrystals.com/CFP2/home_j/home.htmlIQD

http://www.act.co.uk/welcome.html ACT

9.4 Inductors

The VCO inductor value required on the reference design was in the order of 5.6 nH. One of the key specification areas was to maximise 'Q' which prompted the use of the Coilcraft high 'Q' air core inductors. However the Coilcraft 0805CS range did not include a 5.6 nH part so as an alternative an 0603 part from MuRata was used, the LQG11A range. These exhibit lower Q than an 0805 part but are available in much wider range of values between 1 nH and 6 nH and at 1.5 GHz still provide a 'Q' of nominally 70 to 80.

http://www.murata.com/develop/index.htm Data found under Chip-Inductors.

The Coilcraft ranges of inductors were chosen specifically on the grounds of exceptionally high 'Q'. The larger inductors required for the IF2 filter were chosen from an alternative supplier for a smaller package outline. It is strongly recommended that the VCO inductor is chosen to maximise circuit 'Q' and as such an 0805 part should be the target such as the Coilcraft 0805CS range.

http://www.coilcraft.com/0805hq.html	High 'Q' Components for VCO tuning circuit
http://www.coilcraft.com/0805cs.html	Lower 'Q' equivalent
http://www.coilcraft.com/1008cs.html	Recommended IF1 filter components.

Toko inductors were used for the IF2 filter the data for which can be found at the following websites. These inductors were chosen over coilcraft on the grounds of maintaining high 'Q' but in a smaller package outline than the Coilcraft equivalent.

http://www.tokoam.com/Main Web Page

http://209.186.127.176/passives/inductors/chip_inductors/product.asp?productID=FSLU2520

9.5 Filters

There are two choices for the RF band-pass filter used in the reference design, either a SAW filter or Ceramic filter. The SAW filter is certainly smaller and provides better performance in terms of outband attenuation and usually insertion loss. However dramatic cost reduction is possible by using a ceramic filter especially when more than one part is required. The ceramic filter provides a perfectly good solution but does rely heavily on adequate package grounding to maintain its insertion loss properties. In the reference design provision was made for both filter types but in final production only one footprint should be used to allow optimal layout.

MuRata Ceramic Bandpass Filter 1.5754 GHz:DFC21R57P002HHC

At the time of writing, the data sheet for the MuRata filter could be found using the search engine at either one of the following websites by simply entering the part number above.

http://www.murata.co.jp/search/pn-e.html

http://www.murata.com/develop/index.htm

Mitsubishi SAW Filter 1.5754 GHz: MF1012S-1

http://www.mitsubishichips.com/data/datasheets/hf-optic/saw02.htm Data Sheet Listed

http://www.mitsubishichips.com/products/microwave/saw/index.html Products Index Page.

9.6 GPS Active and Passive Antenna

For the reference design a wide range of active antenna could be used with gains ranging from 13 dB to 26 dB. Most typical antenna are rated at 5 V, except for SiGEM, which exhibit a wide operating range between 3 and 5 V. To achieve optimal performance with a passive antenna solution the antenna element should ideally yield gains in the order of +5 dBi at the zenith. In order to do this the ground plane dimensions play a very big part in the design.

9.6.1 Active GPS Antenna

The reference design has been tested with a number of typical active GPS antennae intended for automotive applications. The various types are listed here together with links to data information.

SiGEM

SGM3900P	Vcc = 3 V to 5 V	Gain = 28 dB
SGM3902P	Vcc = 3 V to 5 V	Gain = 13 dB
Website:	http://www.sigem.ca/products/index.htm	

Matsushita Electric Works

GPS-F-26-SMA-01-B	Vcc = 5 V	Gain = 26 dB
Website:	http://www.mew.com/home.html	

Micropulse

13800	Vcc = 5 V	Gain = 20 dB to 26 dB
Website:	http://www.micropulse.com/catalog.htm	

9.6.2 Passive Antenna Elements

In order to implement a passive patch GPS antenna the reference design would have to be altered to incorporate both on chip LNA's of the UAA1570. This approach is the most difficult in that the antenna gain has to be optimised to achieve desired system performance. To this end a reasonably sized ground plane is required which often goes against the size constraints of the project. For information a couple of choices are suggested here.

Alpha Industries (Trans-Tech)

The antenna are actually produced by Trans-Tech, a subsidiary of Alpha Industries. As such the Alpha website does not provide data on line but pointers to contacts. All their elements are specified at 4.5 dBi typical and are based on ground planes of between 50 mm and 70 mm square. The ground plane arrangement can alter the centre frequency of the element so much care is required in adequately tuning and optimising antenna gain in a given design.

PA25D21580PN	25 mm Ceramic Patch
PA50D91575NN	50 mm Ceramic Patch
Website:	http://www.alphaind.com/advscripts/products/product/Antennas.asp

9.7 Eezmatch Software

The Eezmatch software was used to allow the matching networks for the RF stages to be designed. This software is inexpensive, and can be obtained from Besser Associates as detailed (see Reference [5]).

10 REFERENCES

[1] Data Sheet UAA1570HL
Global Positioning System (GPS) Front-end Receiver Circuit
12nc 9397 750 04463

[2] Data Sheet SAA1575HL
Global Positioning System (GPS) Baseband Processor
12nc 9397 750 06055

[3] Users Manual
User Interface Manual for the EXACT GPS Chip-Set (Version 1.2)
SNA/UM98008

[4] Handbook of Filter Synthesis
Author: Anatol I Zverev
Published by John Wiley and Sons, Incorporated 1967
Library of Congress Catalog Card Number:67-17352

[5] Eezmatch Student Edition, Version 1.3.0.1, Besser Associates, 4600 El Camino Rsal, Suite 210, Los Altos, CA94022,
Telephone 415 949 3300.
Website: http://www.bessercourse.com

APPENDIX A

Netlist for first IF filter used on the reference design for SPICE simulation. This netlist is a single sided equivalent of the circuit implemented on the PCB itself to aid simulation.

```
/* First IF Filter for UAA1570 at 41.82MHz
circuit;
/* DC Supply */
e_supply(VCC,GND)supply;

/* IF signal inputs */
e_if1(INP,GND);

/*Resistors  */
r_1(MX1P,GND)454;
r_2(INP,GND)6k;

/*Capacitors*/
c_1(INP,GND)72p;
c_2(INP,1)6.8p;
c_3(1,GND)72p;
c_4(MX1P,GND)78p;
c_5(1,MX1P)8.2p;

/*Inductors*/
l_1(1,GND)165n;
l_2(MX1P,GND)165n;
l_3(INP,GND)180n;

ground: GND;

/*Calculate loop gain*/
LG = (vn(MX1P)/vn(INP));
end;

nodelist;
ac;
supply=5;
 f=gn(1000k, 1000000k, 2000);
 e_if1 = sw(0.1,0);
 file: dbpha(vn(INP)), dbpha(vn(MX1P)), dbpha(LG);
 file: vn(INP), vn(MX1P);
end;
run;
```

APPENDIX B

Netlist for second IF filter used on the reference design for SPICE simulation. This netlist is the single sided circuit actually implemented on the PCB itself.

```
/* Second IF Filter for UAA1570 at 3.48MHz
circuit;
/* DC Supply */
e_supply(VCC,GND)supply;

/* IF signal inputs */
e_if1(INP,GND);

/*Resistors*/
r_1(MX2P,GND)820;
r_2(INP,GND)2.2k;

/*Capacitors*/
c_1(INP,GND)82p;
c_2(INP,1)47p;
c_3(1,GND)18p;
c_4(MX2P,GND)68p;
c_5(1,MX2P)47p;

/*Inductors*/
l_1(1,GND)22000n;
l_2(MX2P,GND)22000n;
l_3(INP,GND)27000n;

ground: GND;

/*Calculate loop gain*/
LG = (vn(MX2P)/vn(INP));
end;

nodelist;
ac;
supply=5;
 f=gn(10k, 100000k, 1000);
 e_if1 = sw(0.1,0);
 file: dbpha(vn(INP)), dbpha(vn(MX2P)), dbpha(LG);
 file: vn(INP), vn(MX2P);
end;
run;
```